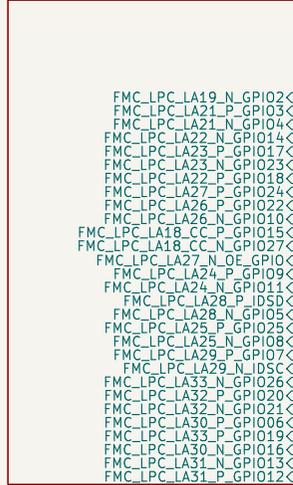


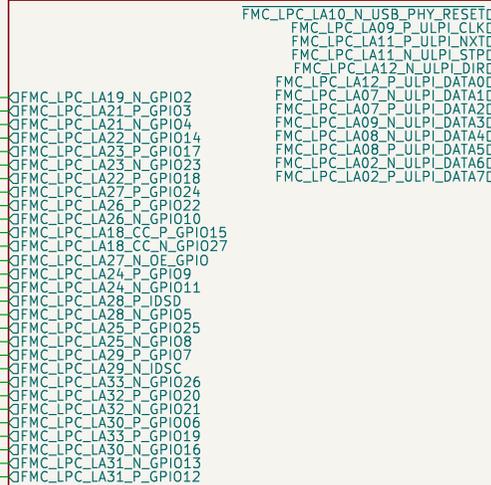
Vinculin FMC TOP

Erreg - Ver 1
 - Decide against a new addition and in VIO Control/Amplify routing

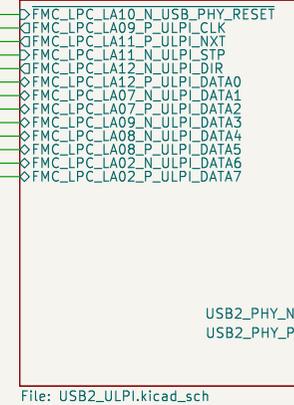
pi_hats



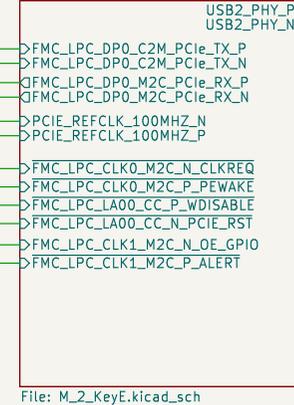
FMC_Conn



USB_2_ULPI



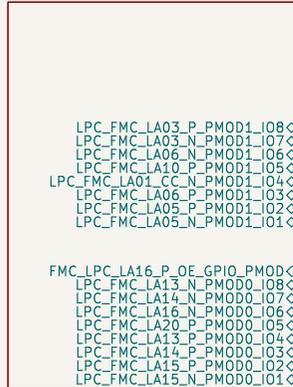
M_2_KeyE



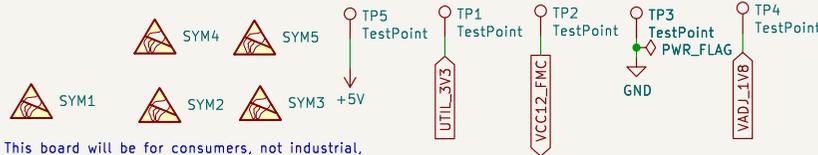
Voltage_Regs



PMODS



Test Points



Refer to page 28, rule 3.25
 All keying holes shall remain electrically isolated from the mezzanine module's circuit ground
 Note, checking with multimeter on board showed that FMC mounting holes are not tied to signal ground. They aren't even tied to each other. They must be Non plated through holes

Mounting Holes for FMC



This board will be for consumers, not industrial, Decide to follow VITA 57.1 for air cooled

Pi Hats, and Digilent PMOD connectors
 FMC for M.2 Key E
 Author: Chance Reimer
ApotheoTech LLC
 Sheet: /
 File: pi_hat.kicad_sch

Title: Vinculin FMC

Size: A4 Date: 2023-05-27
 KiCad E.D.A. 9.0.0

Rev: 1.0
 Id: 1/7

FMC Mezzanine Board Side

Max Power Rail Amperage (Max Exp):

VCC12_SW: 1A
 UTIL_3V3: 2.5A
 VADJ 1.8V: 1A
 VREF_A_M2C: N/A

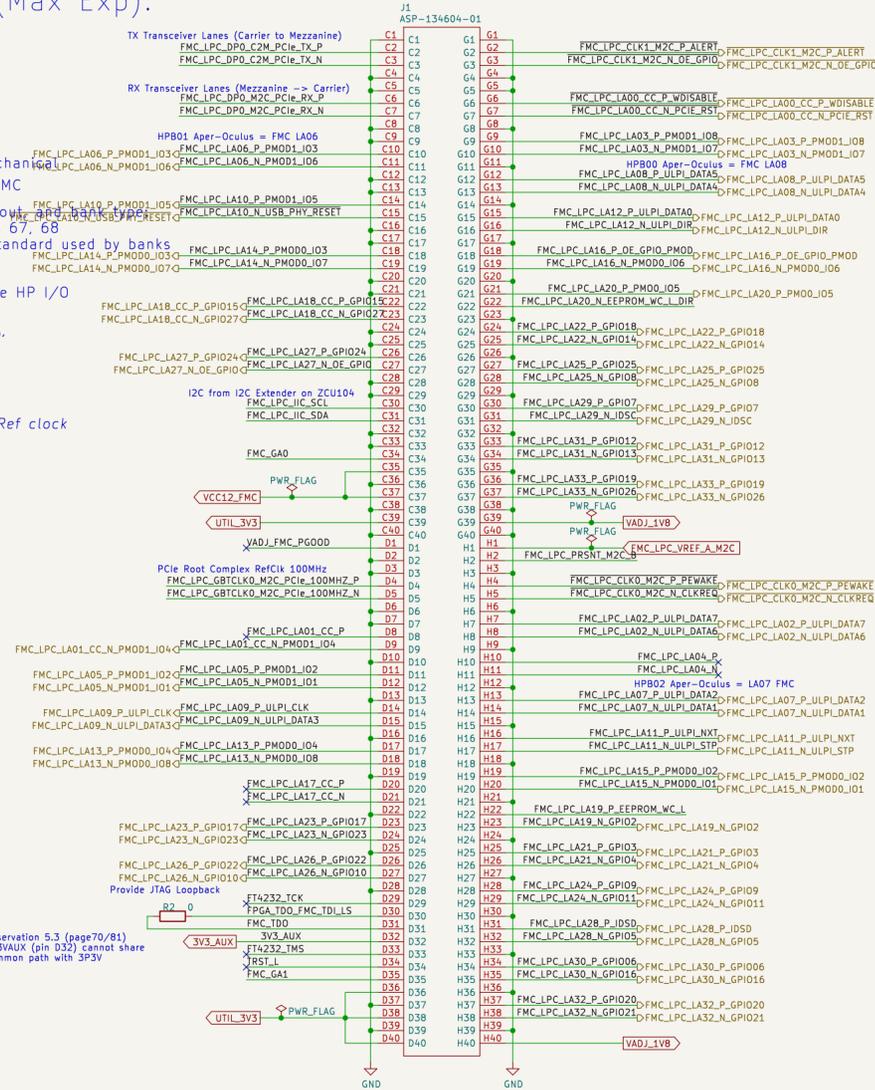
Refer to page 31 of 79 of VITA 57.1 for FMC LPC Mechanism
 Page 28/58 of Schematic for ZCU104 for pinout of FMC

Refer to UG1075 and ZCU104 Schematic for bank pinouts

*On page 6, 7, shows FMC LPC is connected to banks 67, 68
 *Banks are referenced by VADJ_FMC, this is voltage standard used by banks
 *Page 25 of UG1075 for pin definitions of Banks
 *Page 149 of UG1075 has pinout for chip on ZCU104
 *Page 36 of UG1075, shows that banks 66 and 68 are HP I/O

Note --> Page 55 of VITA 57.1
 Rule 5.3, all LA prefix will be associated with Bank A,
 and can use reference voltage pin VREF_A_M2C
 (Note, that stands for Mezzanine to Connector,
 and must have output from board)

Note --> Page 10 of ZCU104 Schematic shows
 FMC_LPC_GBTCLK0_M2C_C_P connects to Transceiver Ref clock
 Pins V8 and V9



Sheet Outputs

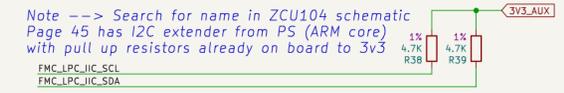
M.2 PCIe Interface

Note --> Page 10 of ZCU104 Schematic shows
 FMC_LPC_DP0_M2C_P/N connects to Transceiver Rx block
 (Pins P4, P3)

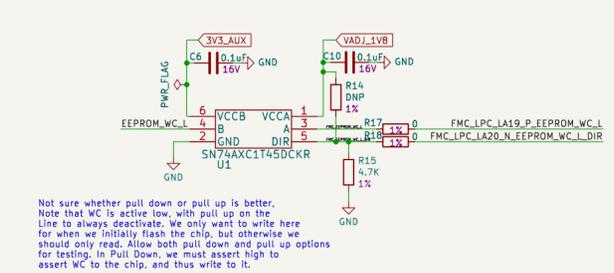
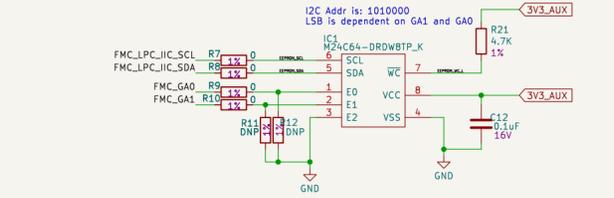
Note --> Page 10 of ZCU104 Schematic shows
 FMC_LPC_DP0_C2M_P/N connects to Transceiver Tx block
 (Pins N6, N5)

FMC_LPC_DP0_M2C_Pcie_RX_P
 FMC_LPC_DP0_M2C_Pcie_RX_N
 FMC_LPC_DP0_C2M_Pcie_TX_P
 FMC_LPC_DP0_C2M_Pcie_TX_N

EEPROM



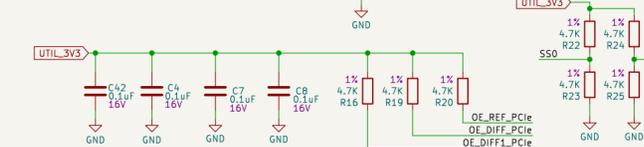
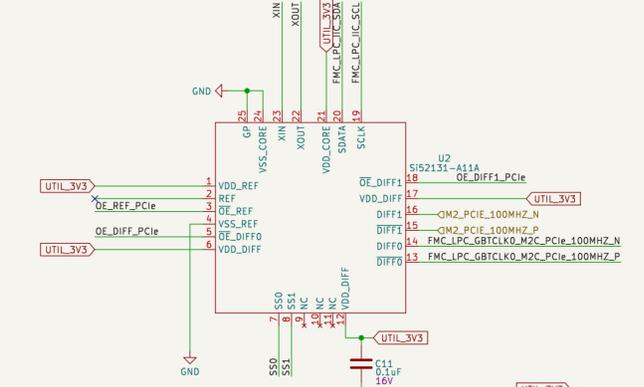
Support FMC IPMI Standard
 - Rule 5.17: EEPROM shall store information contained to info on IO FMC
 - Rule 5.60: EEPROM shall interface with I2C bus signals
 - Rule 5.61: Powered by 3P3VAUX



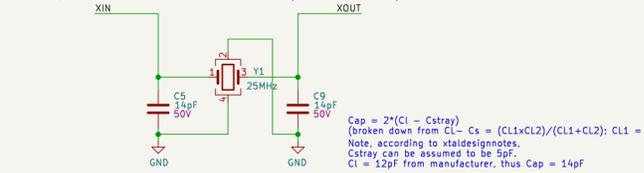
Not sure whether pull down or pull up is better.
 Note that WC is active low, with pull up on the
 line to always deactivate. We only want to write here
 for when we initially flash the chip, but otherwise we
 should only read. Allow both pull down and pull up options
 for testing. In Pull Down, we must assert high to
 assert WC to the chip, and thus write to it.

PCIe Clock Generator

Note --> PCIe Root Complex and Device must
 have synchronous Refclk. Use S152131 to provide
 source to Endpoint and Root Complex

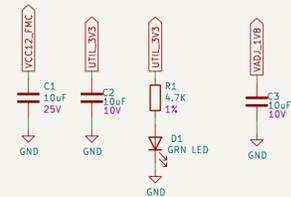


Crystal for PCIe (25MHz)

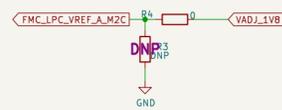


Cap = 2*(Cl - Cstray)
 (broken down from Cl - Cs = (C1+C2)/(C1+C2): C1 = C2
 Note: according to xtldeisignnotes.
 Cstray can be assumed to be 5pF.
 Cl = 12pF from manufacturer, thus Cap = 14pF

Decoupling Capacitors



Note --> Page 70 of VITA 57.1
 Must have VREF_A_M2C meet 0-VADJ.
 Simply have VREF_A_M2C == VADJ
 (Note User Guide page 76 for FMC VADJ values (1.8V nominal)
 (Use pull up resistor for overvoltage errors)



I2C Select Pins (NC)

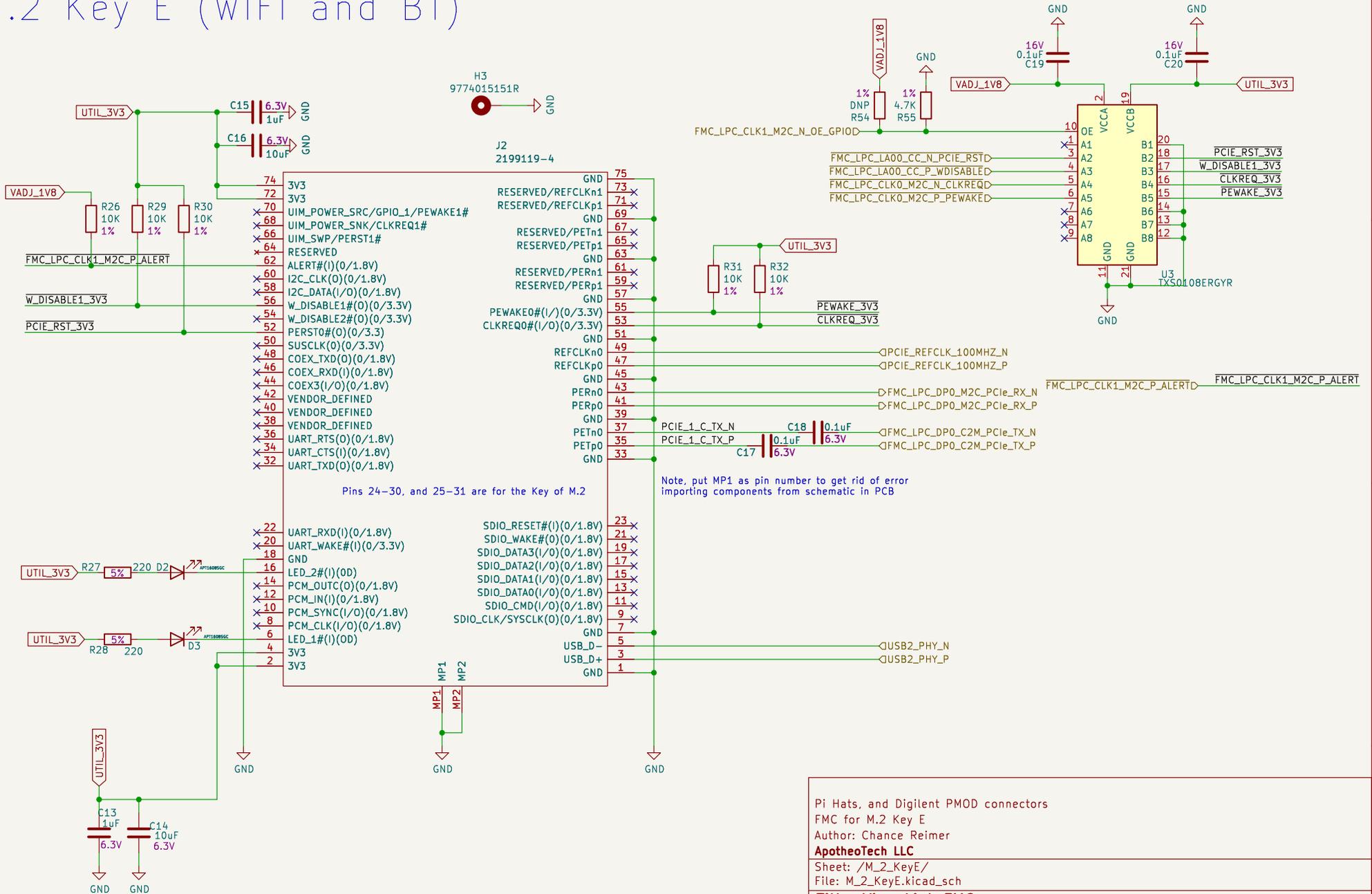
GA[0:1] I2C address select pins
 Not used, driven by carrier, NC

Module Detect Pin

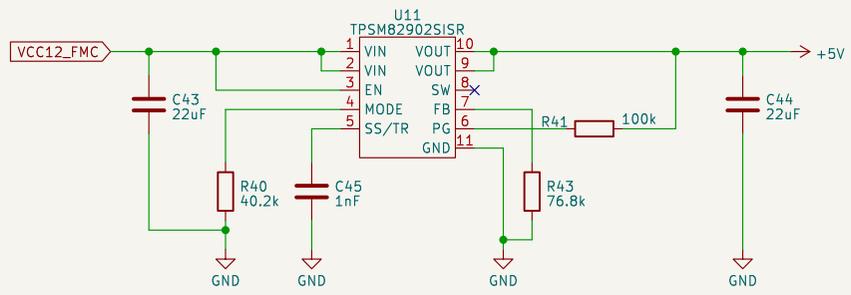


This signal lets carrier know module is present
 (page 48/81)
 Signal is active low (Observation 5.8, page 46/81)

M.2 Key E (WIFI and BT)



Pi Hats, and Digilent PMOD connectors	
FMC for M.2 Key E	
Author: Chance Reimer	
ApotheoTech LLC	
Sheet: /M_2_KeyE/	
File: M_2_KeyE.kicad_sch	
Title: VincuLink FMC	
Size: A4	Date:
KiCad E.D.A. 9.0.0	Rev: 1.0
	Id: 3/7



Pi Hats, and Digilent PMOD connectors

FMC for M.2 Key E

Author: Chance Reimer

ApotheoTech LLC

Sheet: /Voltage_Regs/

File: volt_regs.kicad_sch

Title: VincuLink FMC

Size: A4

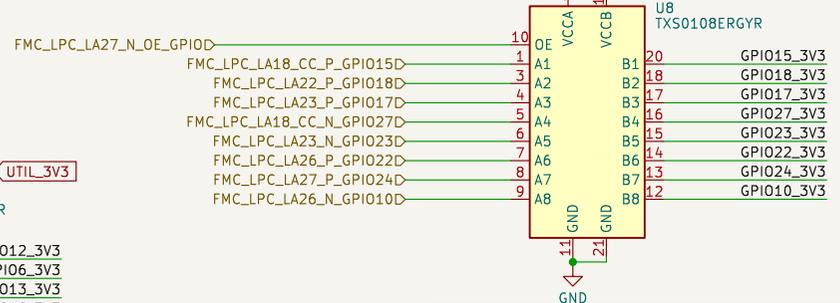
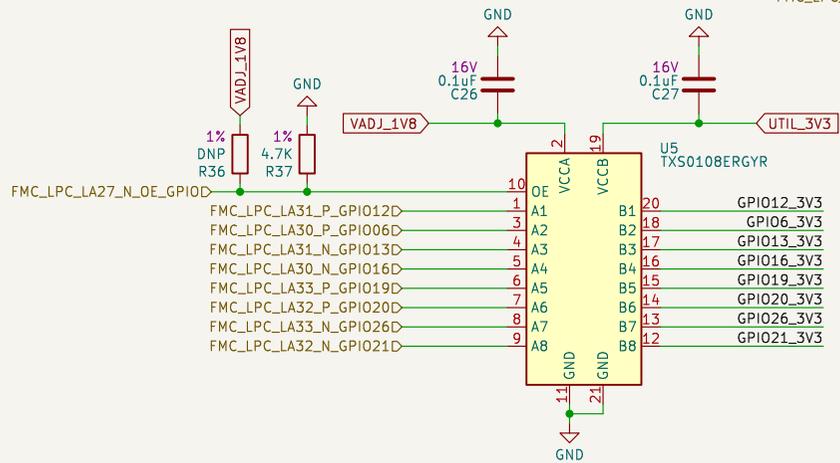
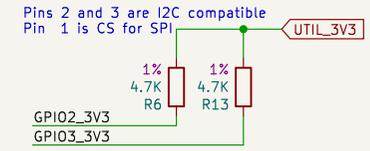
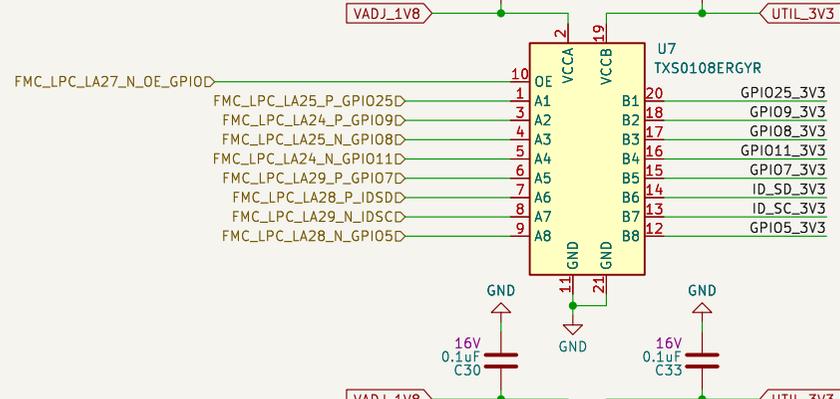
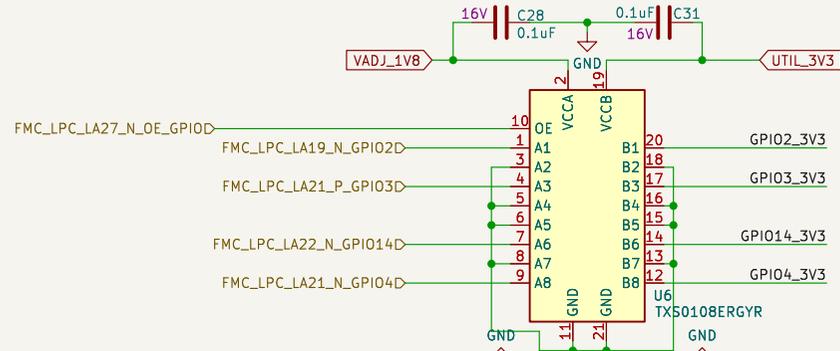
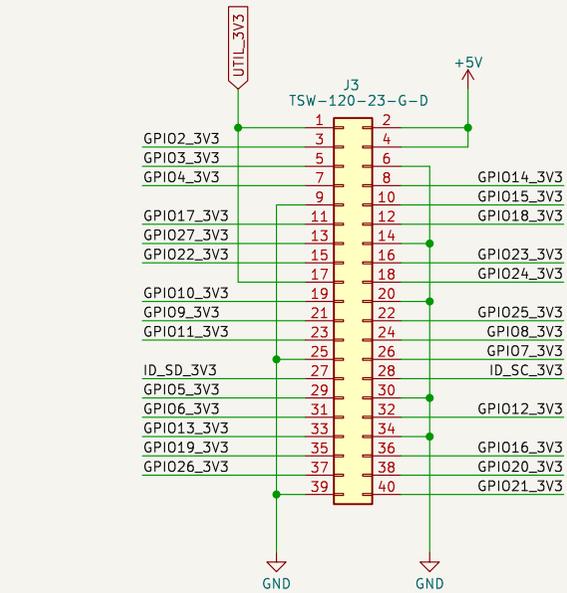
Date:

Rev: 1.0

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Id: 5/7

Pi Hat



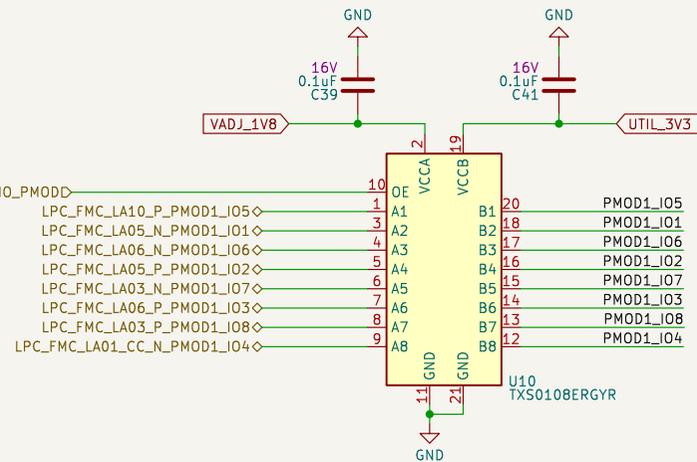
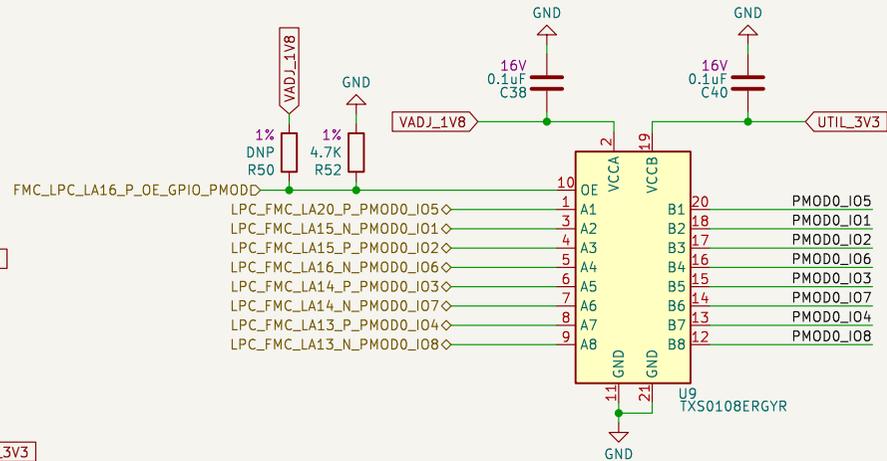
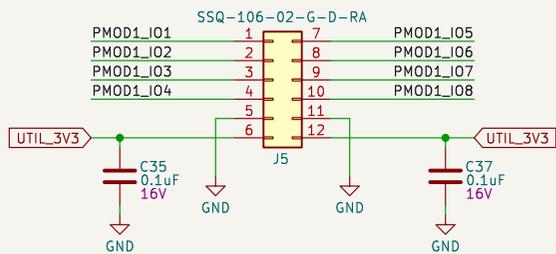
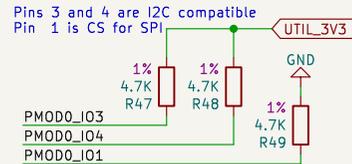
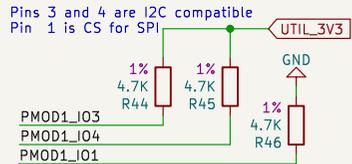
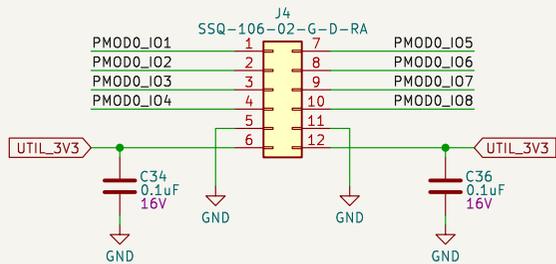
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 Sheet: /pi_hats/
 File: pi_hats.kicad_sch

Title: VincuLink FMC

Size: A4	Date:	Rev: 1.0
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PMODS

16 pins of FMC utilized for x2 PMOD



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Rev: 1.0
 Id: 7/7