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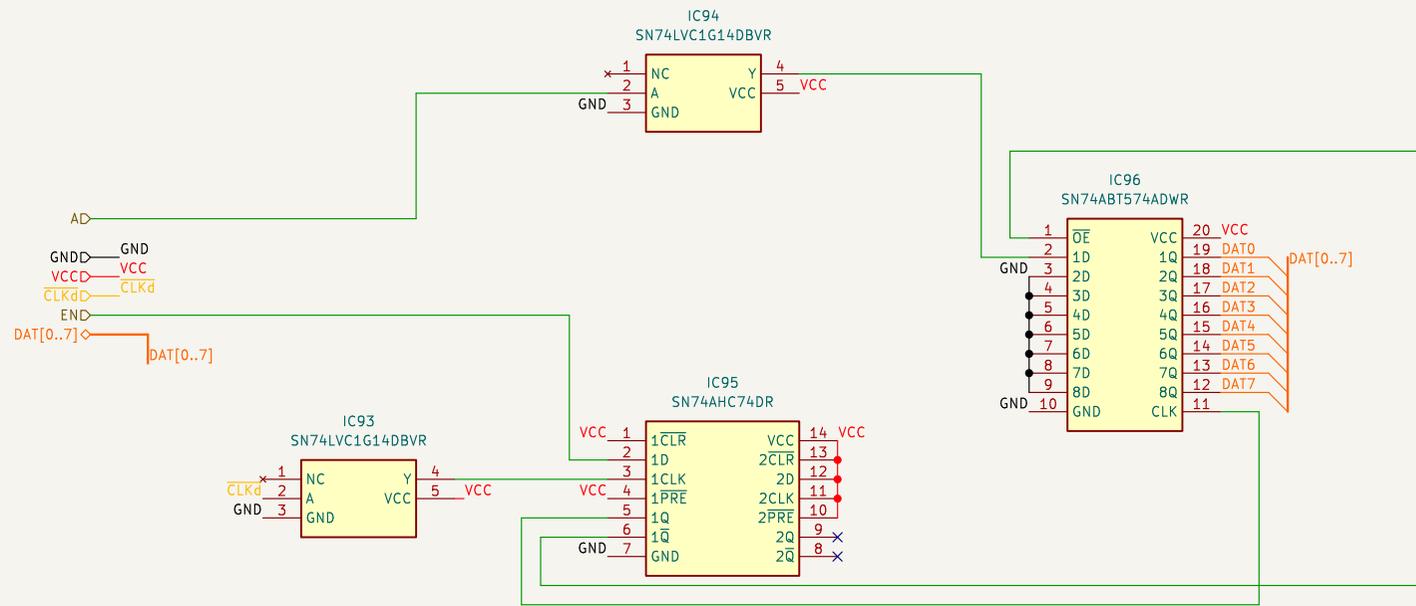
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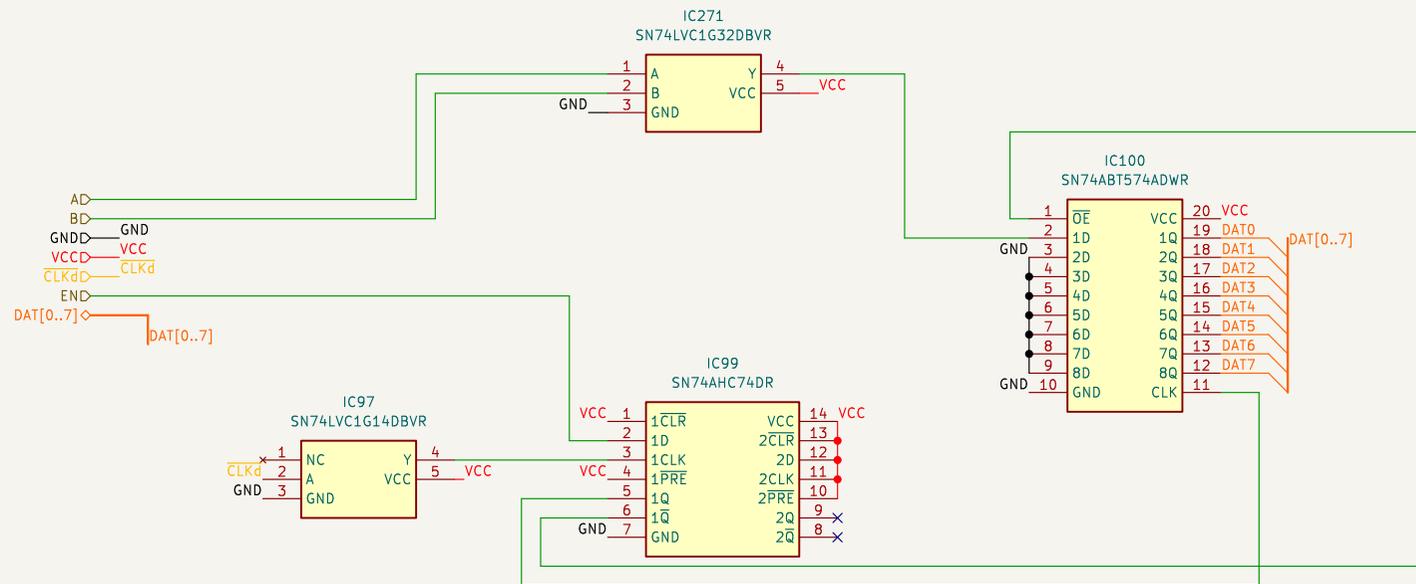
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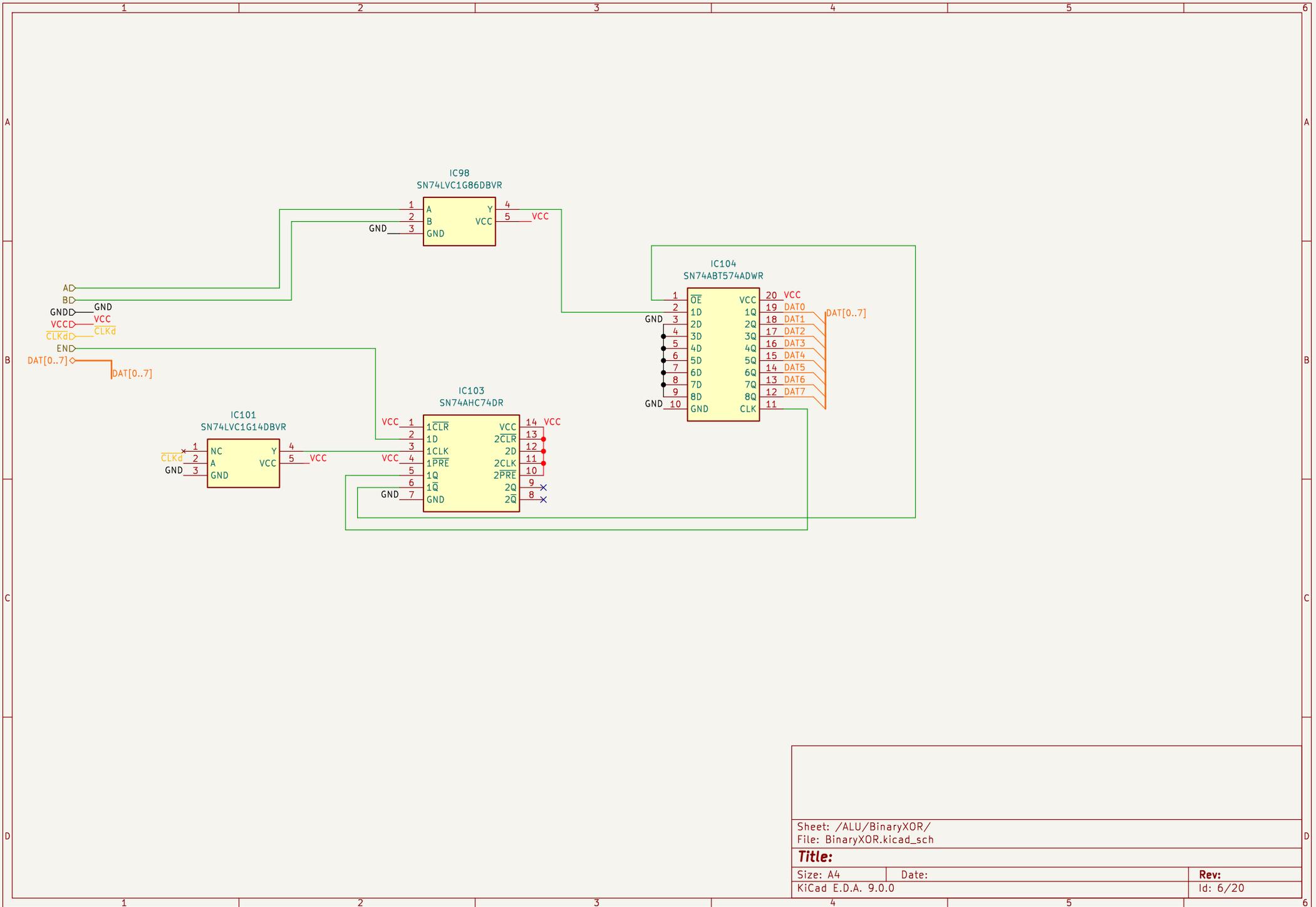
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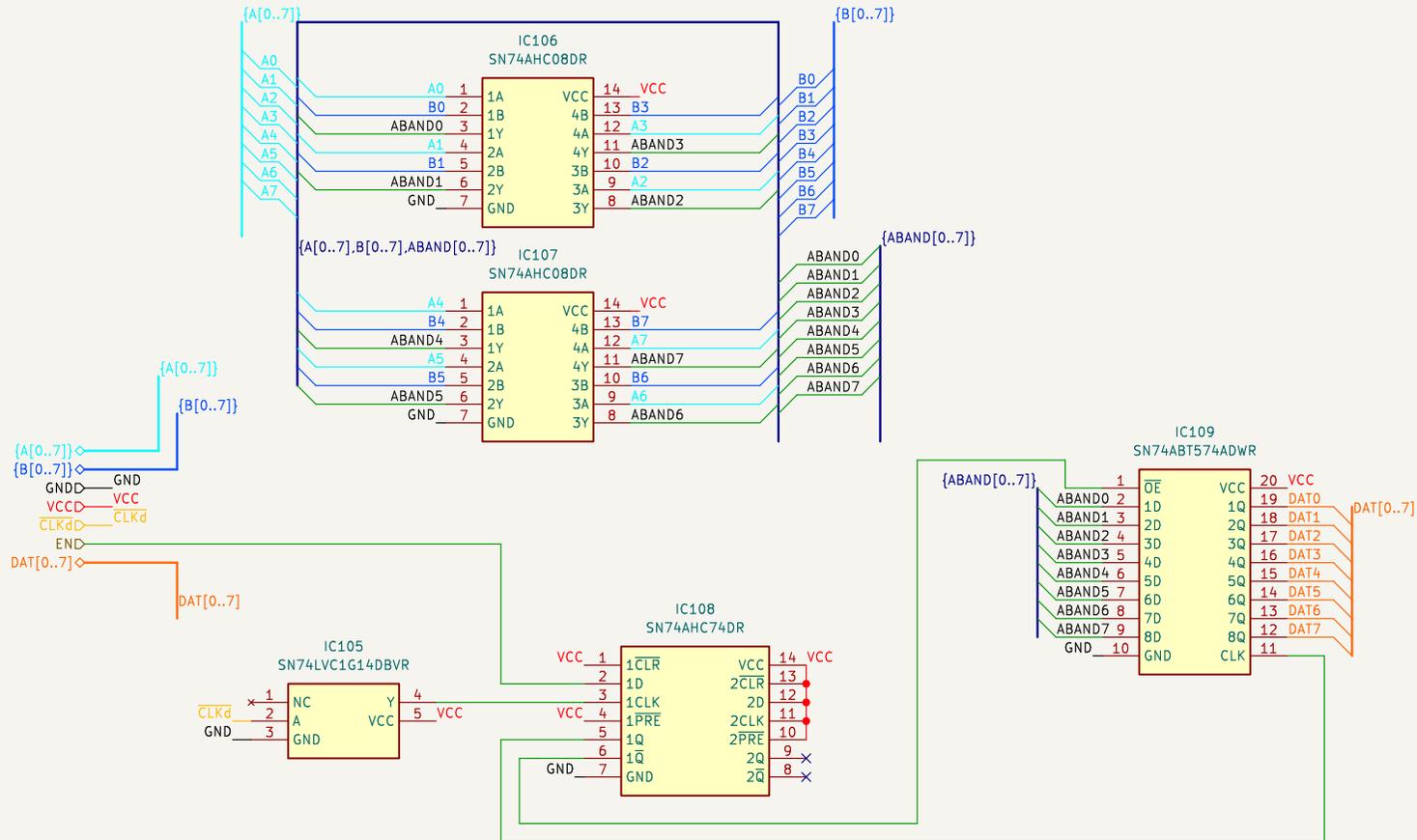
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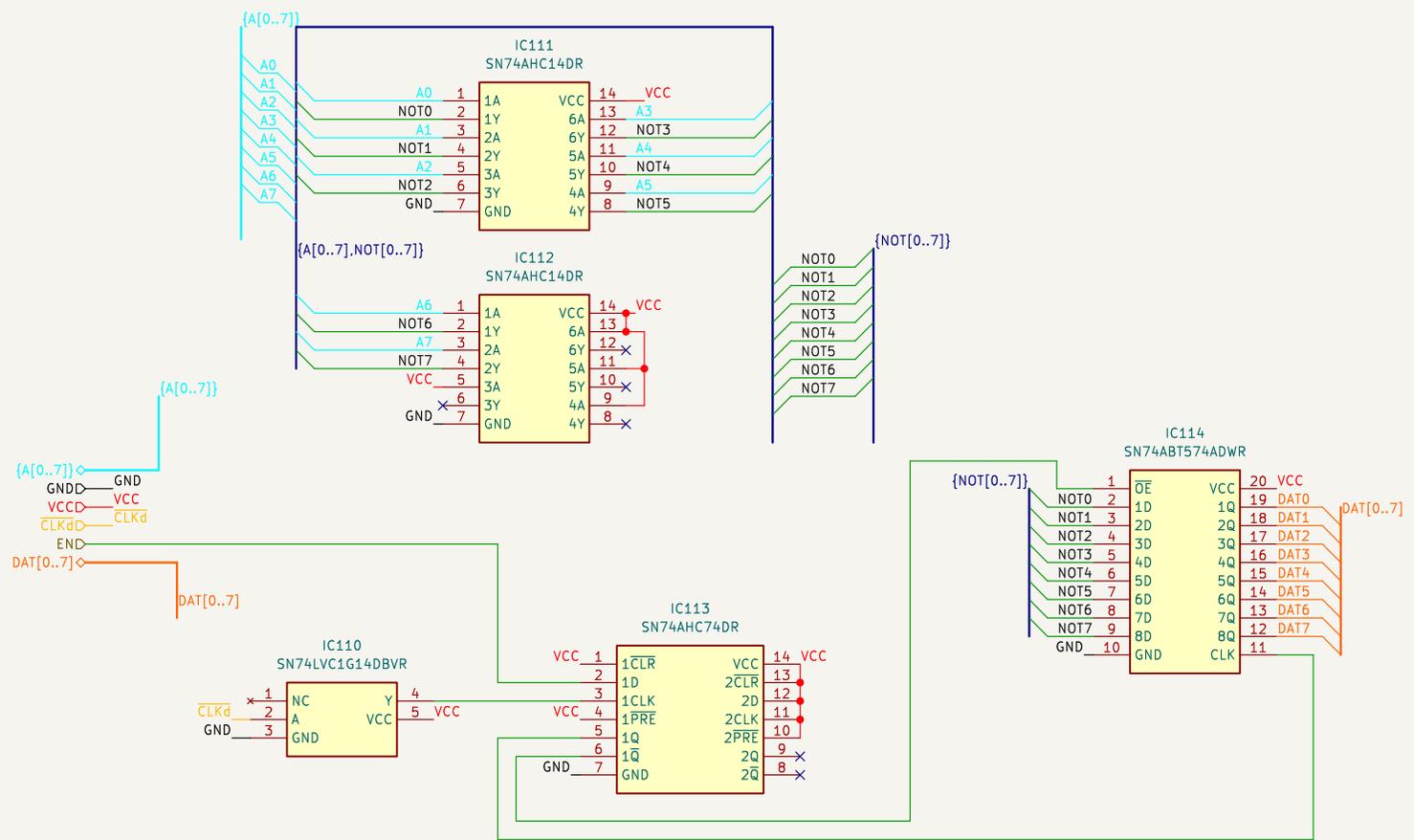
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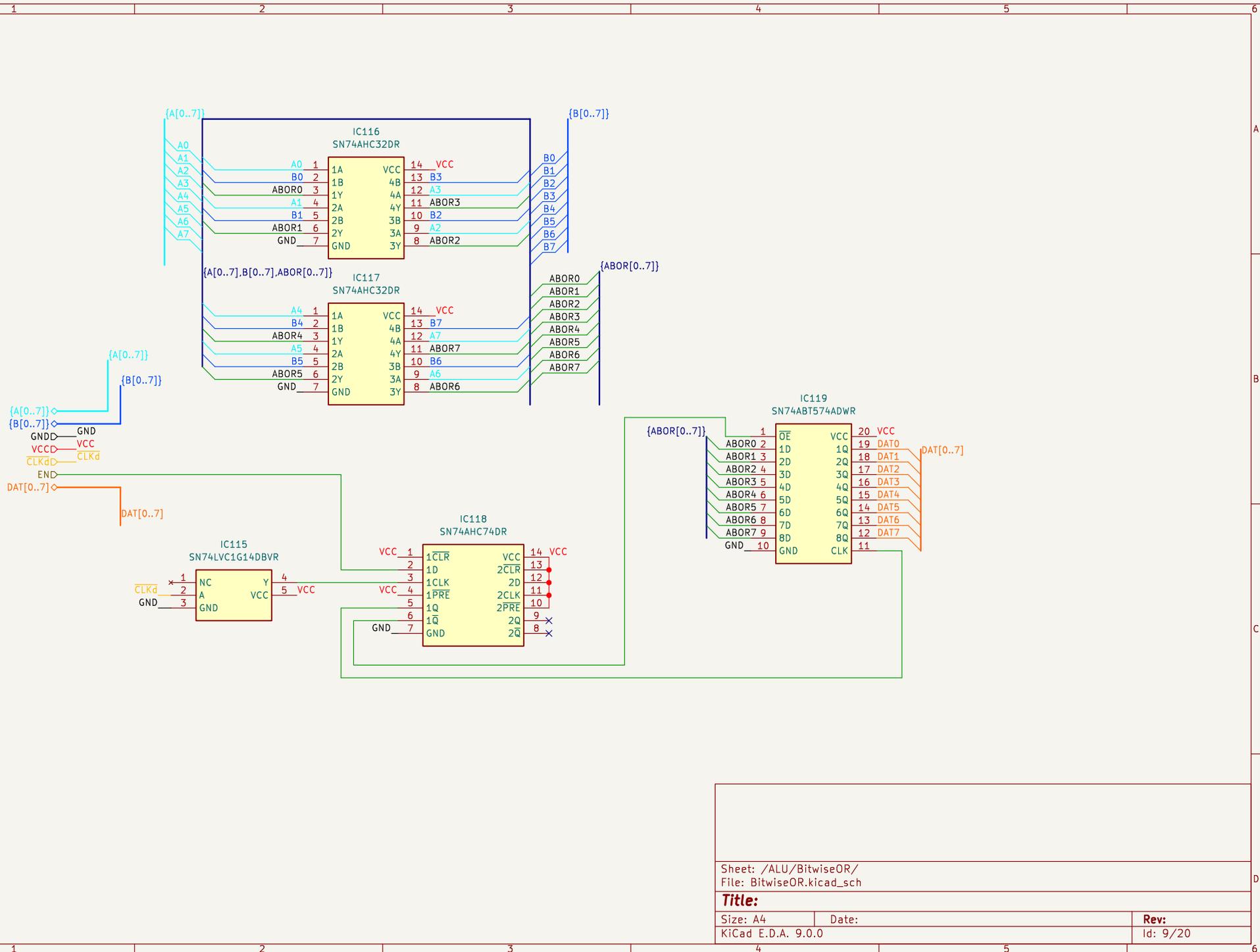
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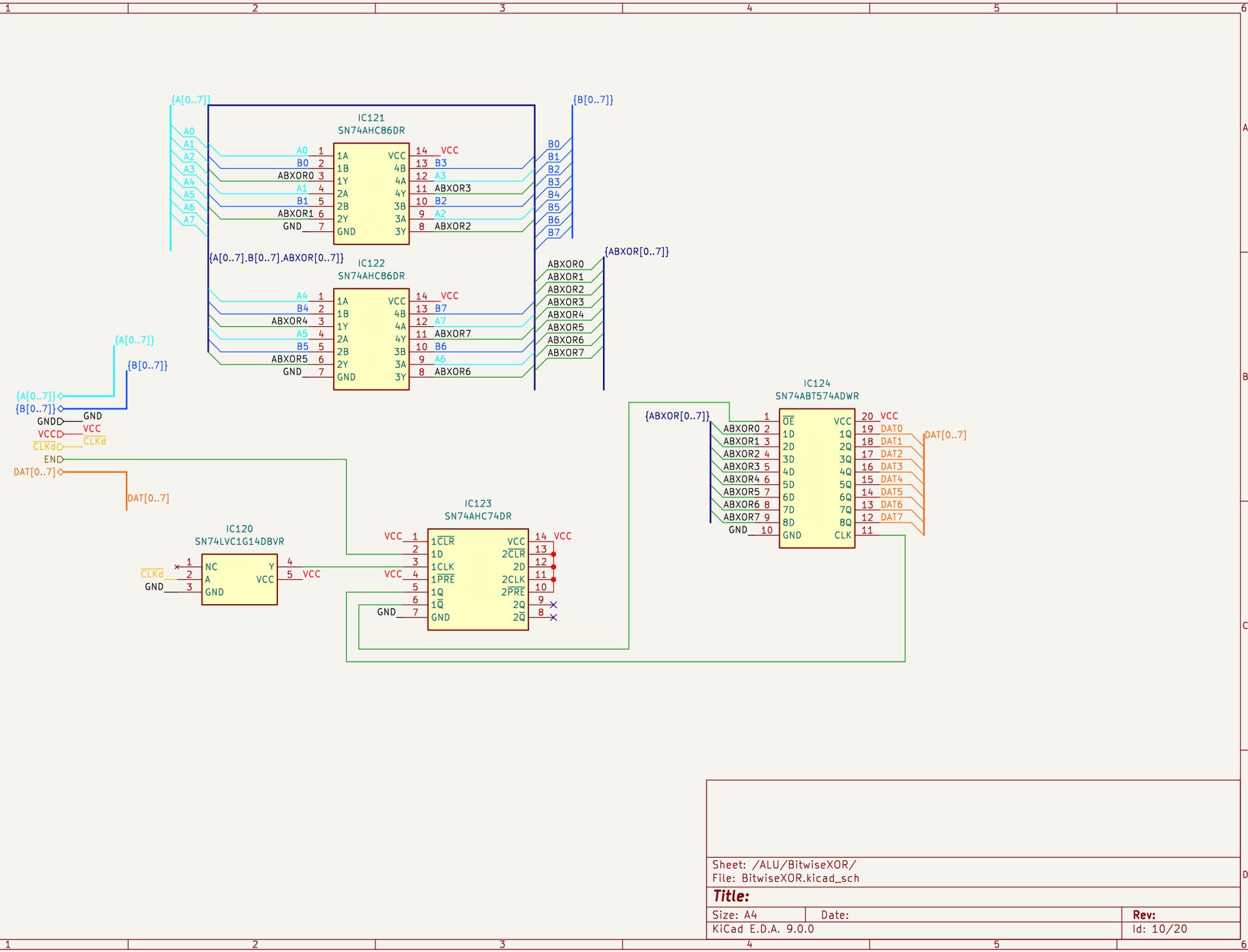
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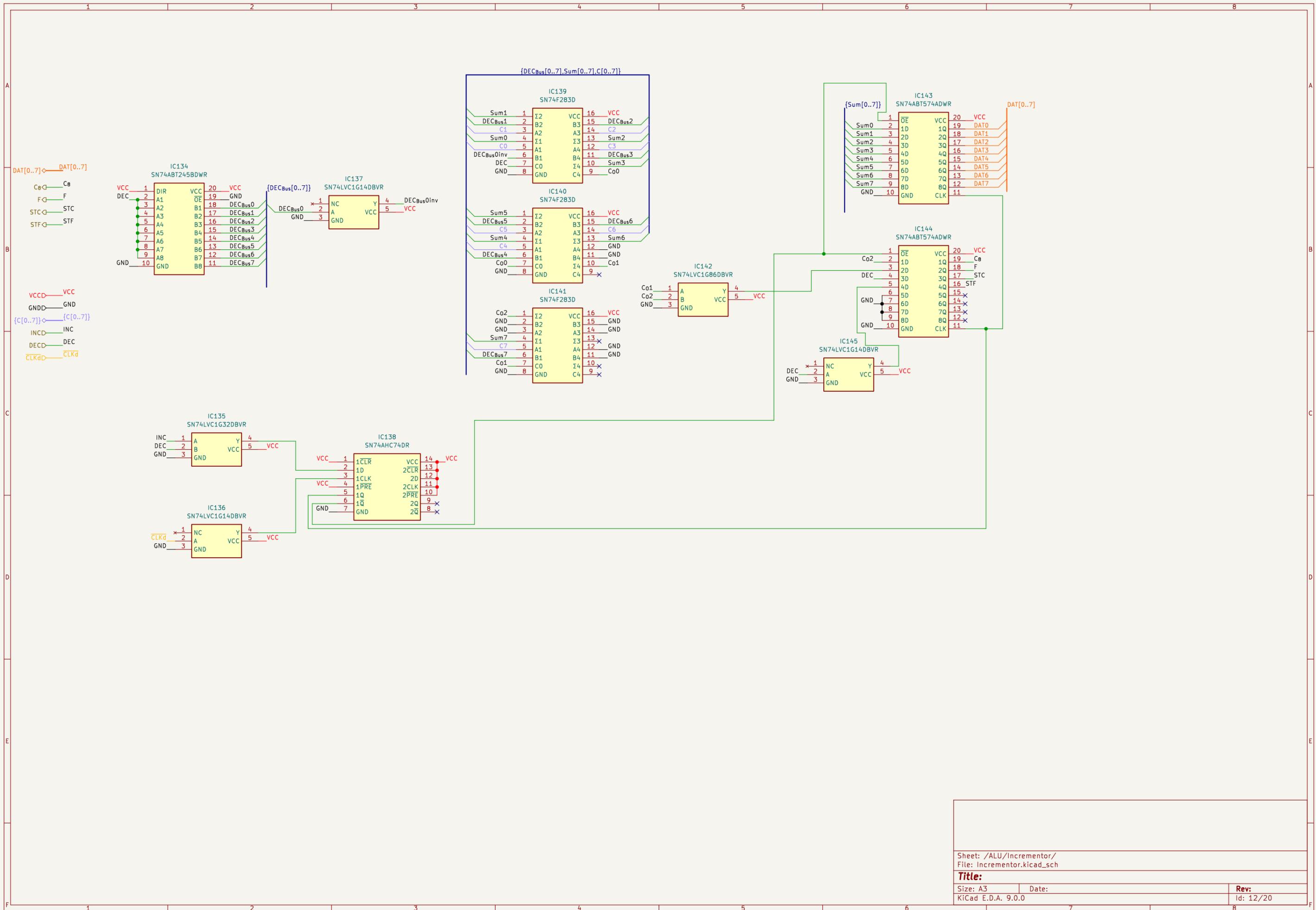
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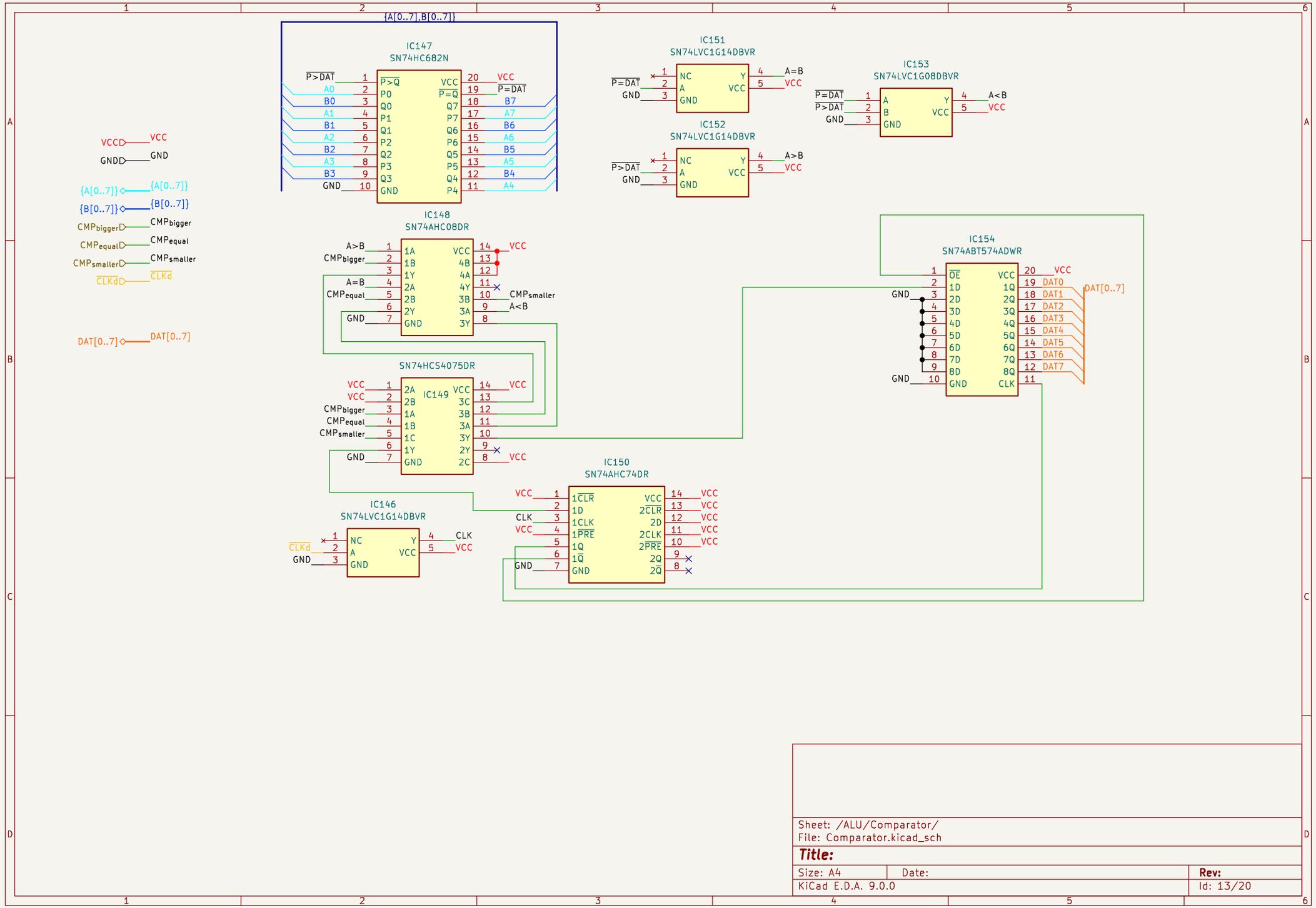
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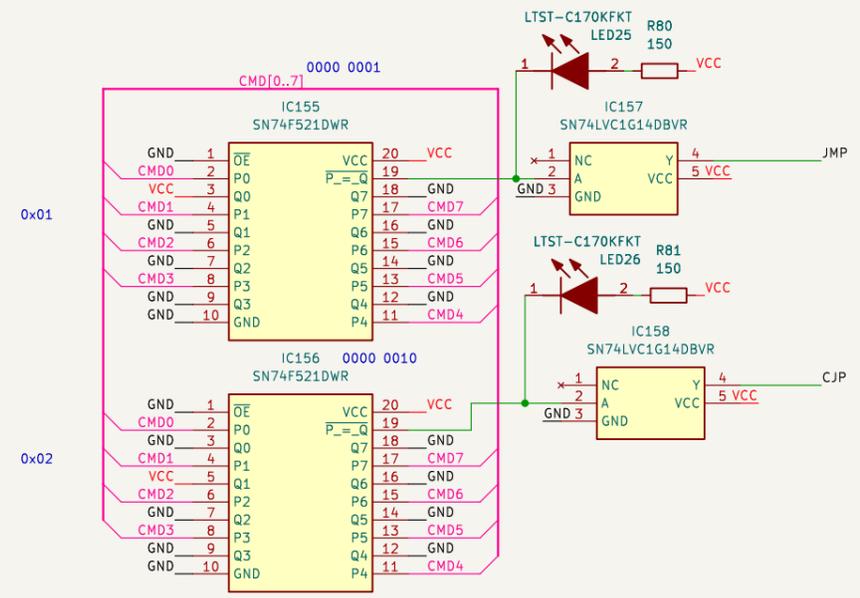
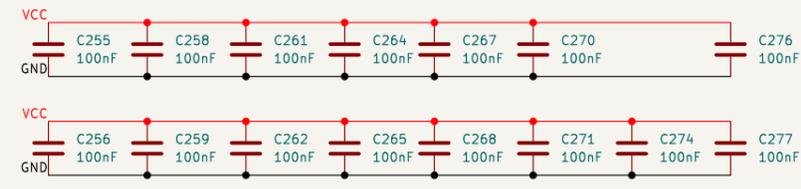
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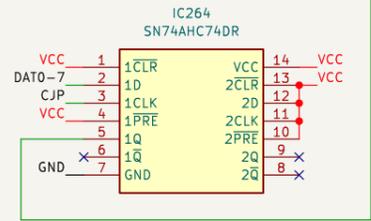
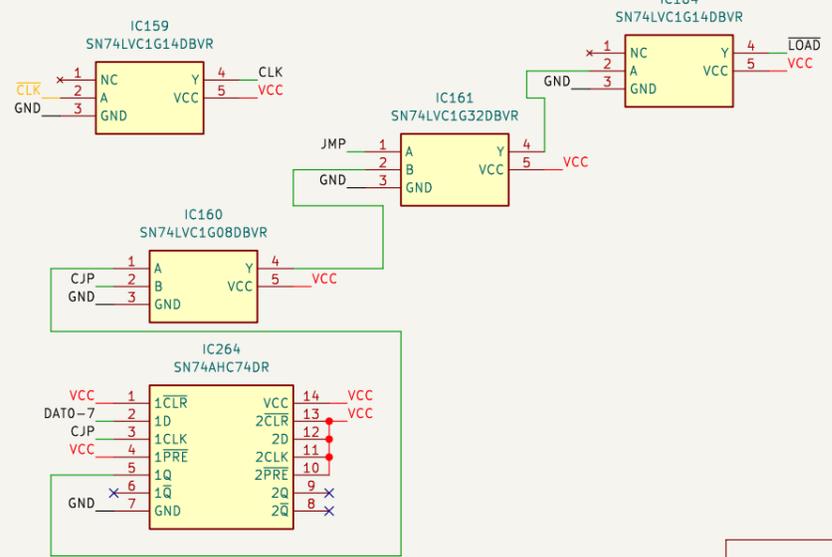
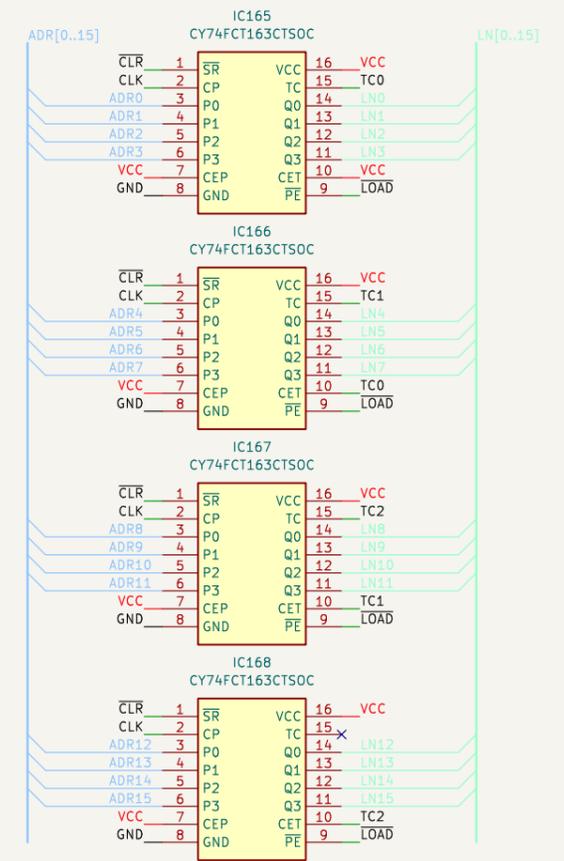
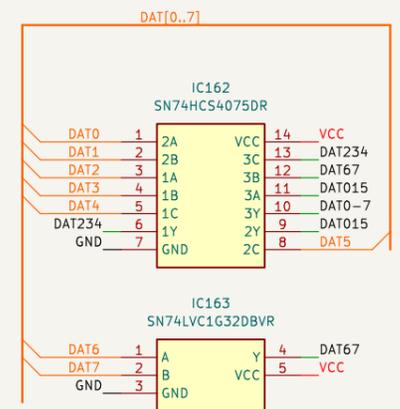
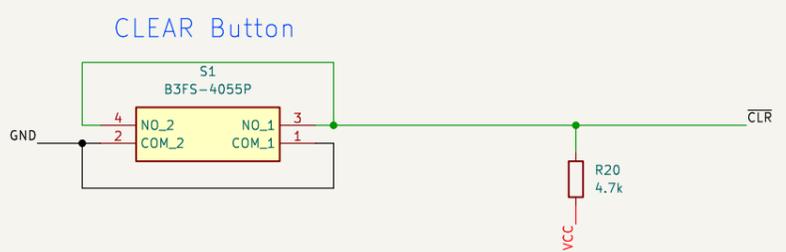
LN[0..15] ◊ LN[0..15]
 GND ◊ GND
 VCC ◊ VCC
 DAT[0..7] ◊ DAT[0..7]
 ADR[0..15] ◊ ADR[0..15]
 CLK ◊ CLK
 CMD[0..7] ◊ CMD[0..7]

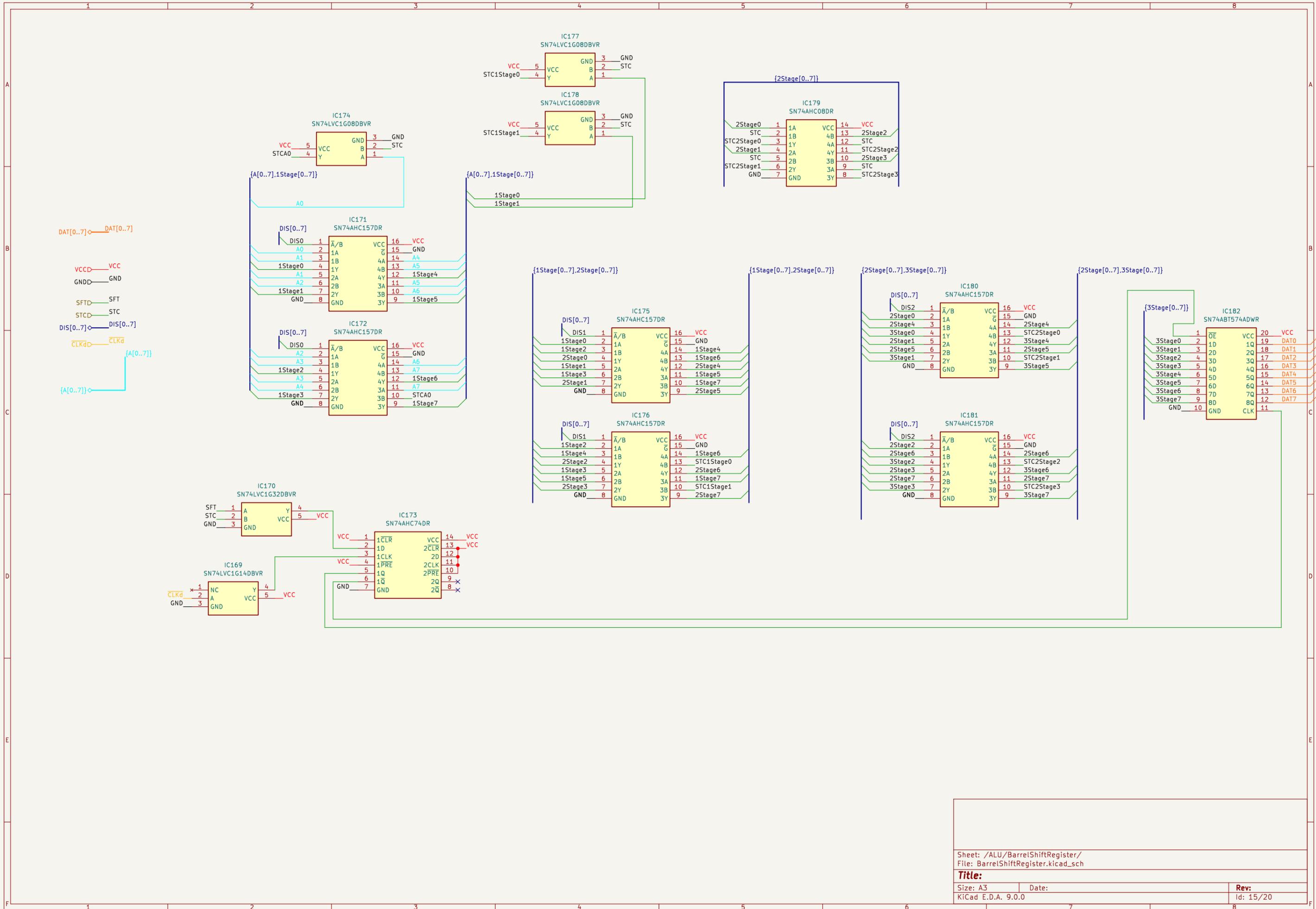


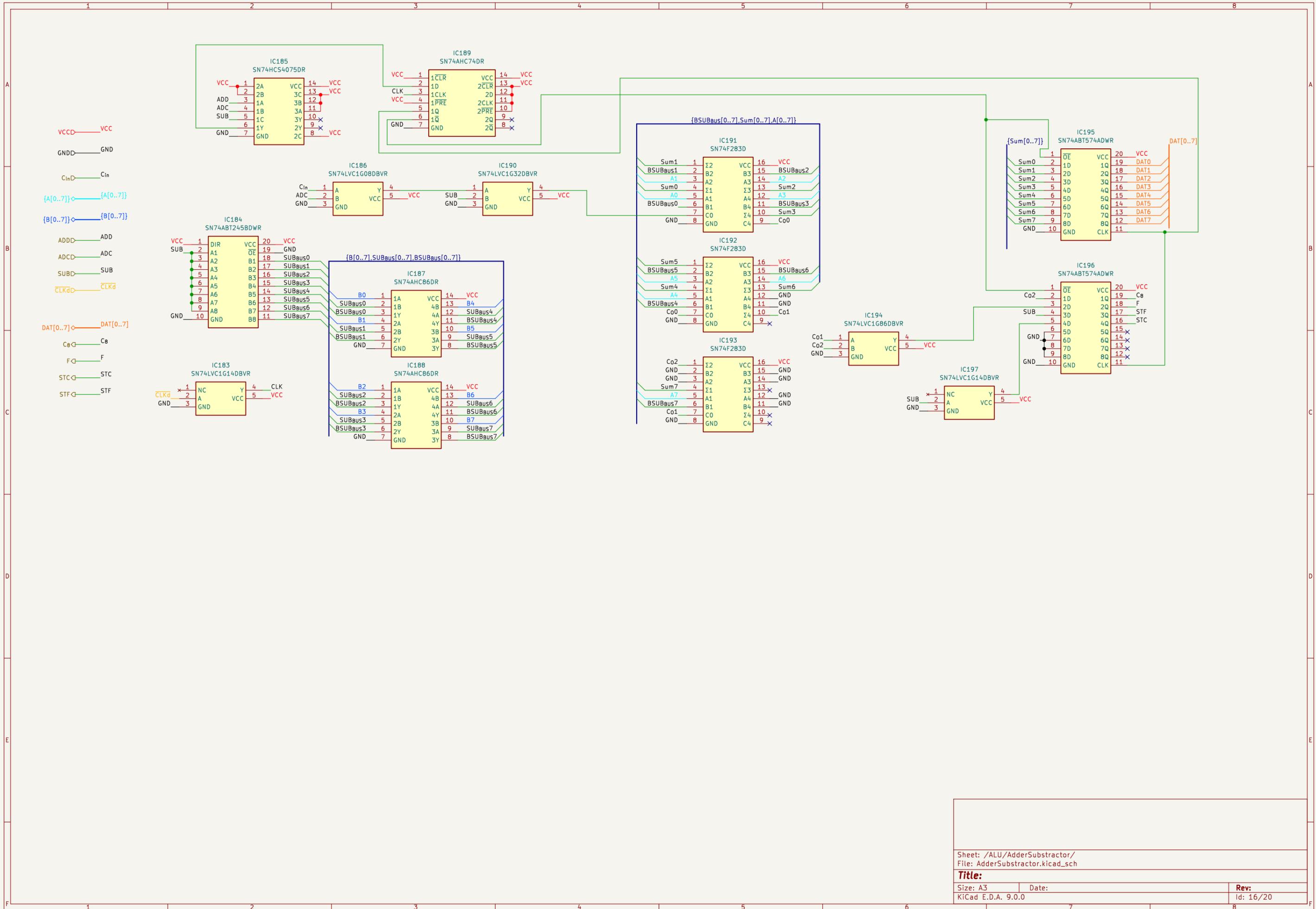
FUNCTION TABLE

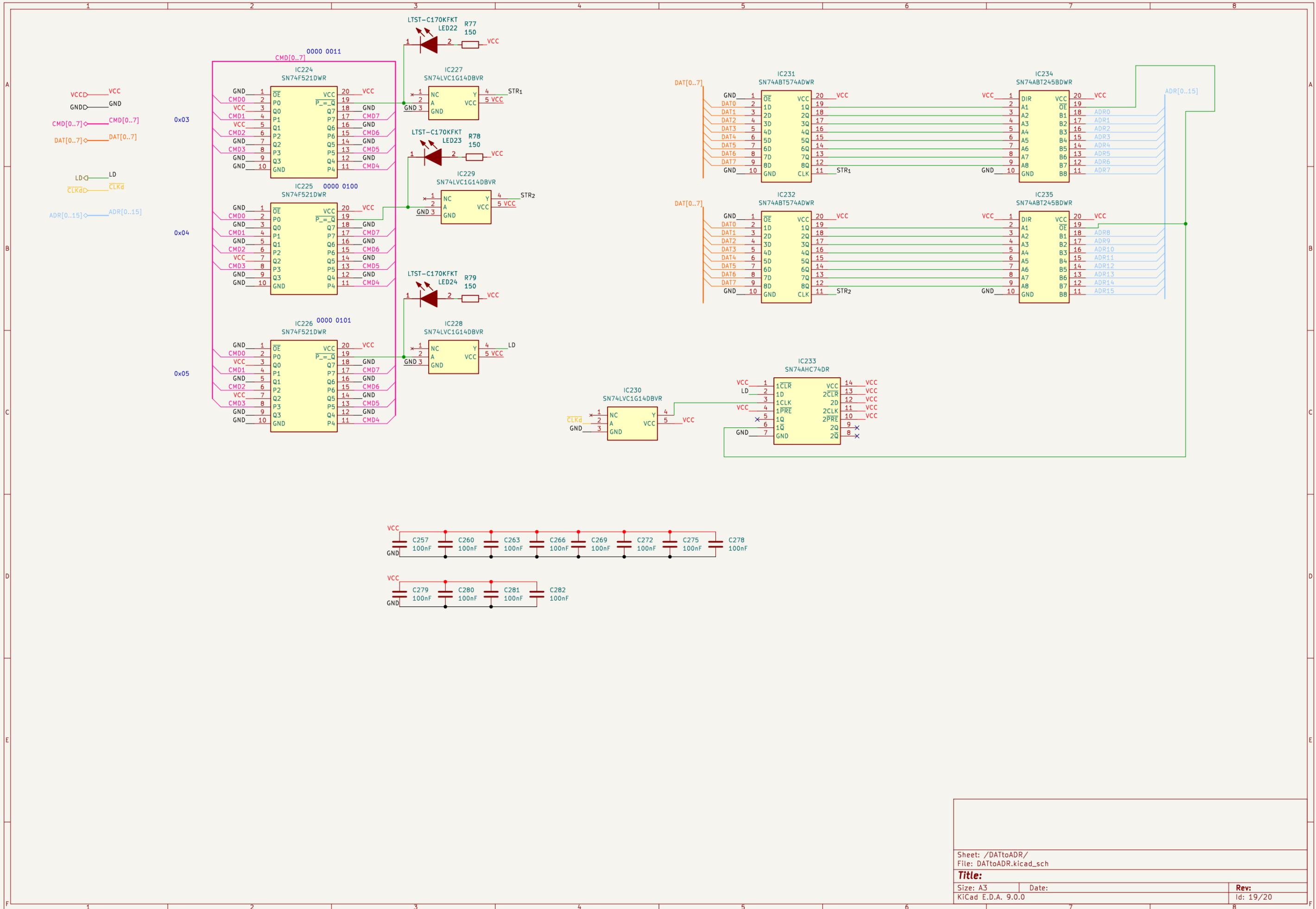
INPUTS				ACTION ON THE RISING CLOCK EDGE(S)
SR	PE	CET	CEP	
L	X	X	X	Reset (clear)
H	L	X	X	Load (P _n → Q _n)
H	H	H	H	Count (incremental)
H	H	L	X	No change (hold)
H	H	X	L	No change (hold)

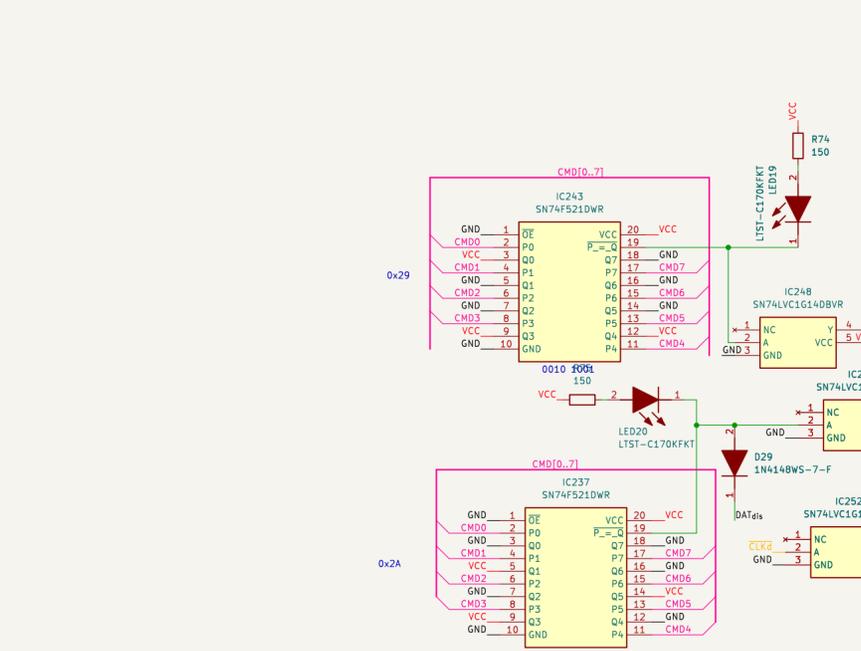
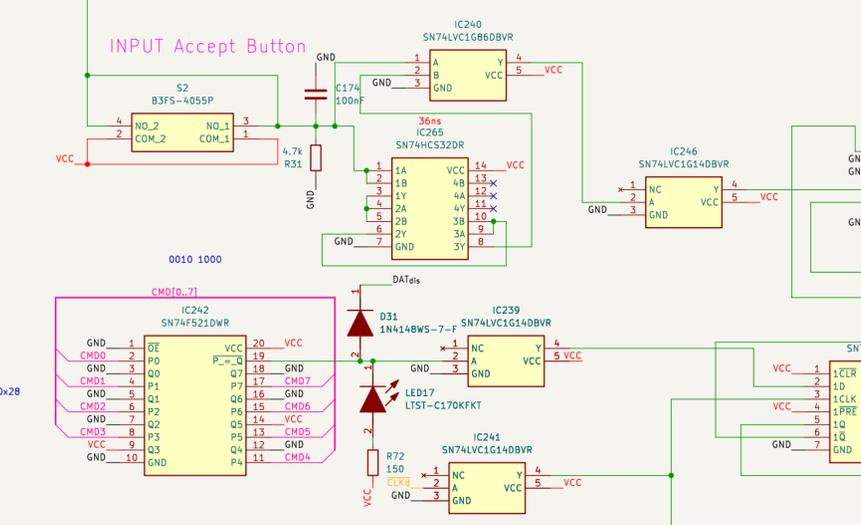
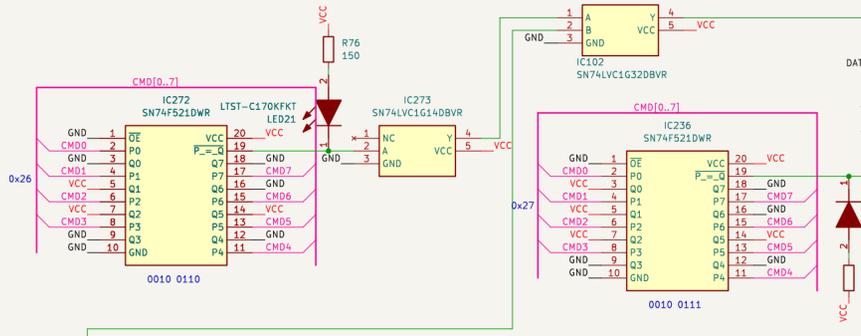
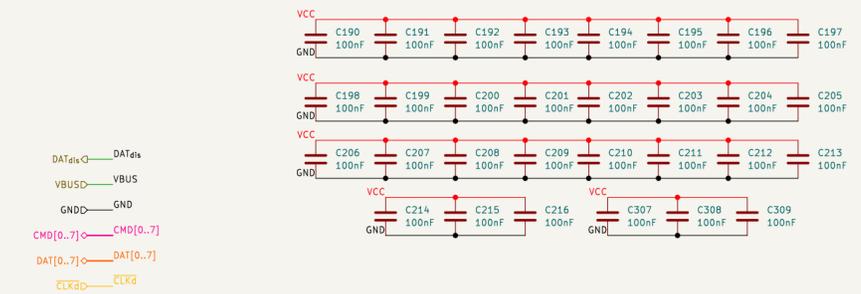
H = High logic level, L = Low logic level, X = Don't care



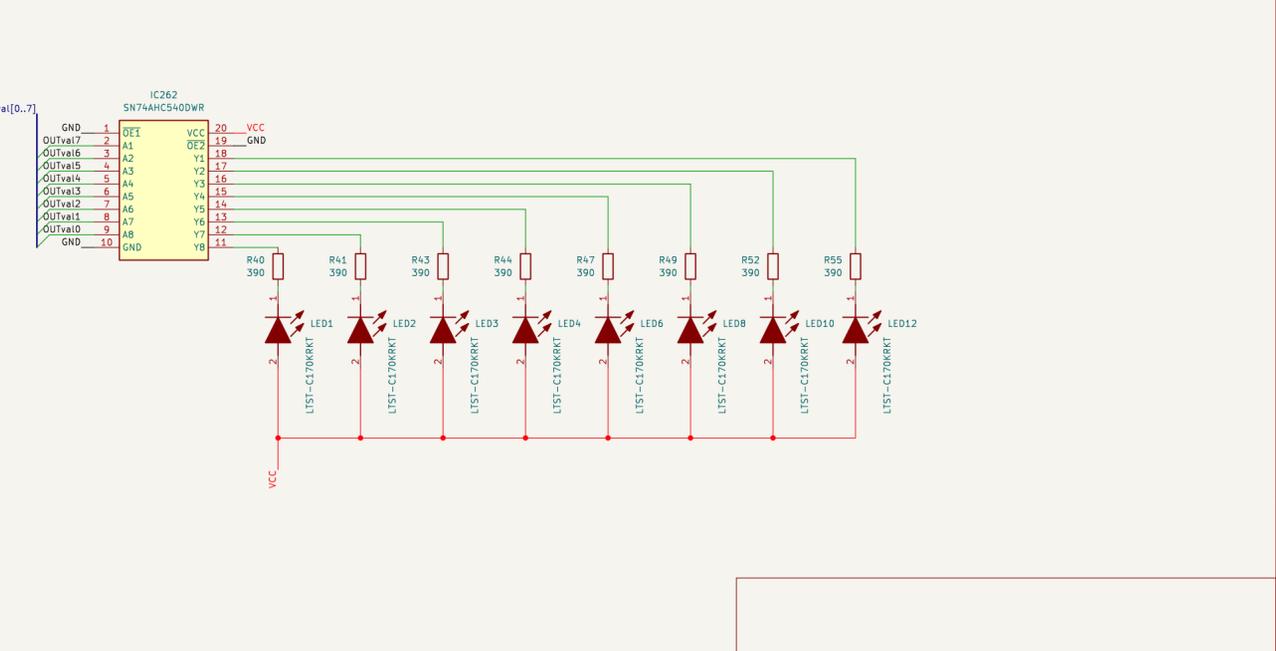
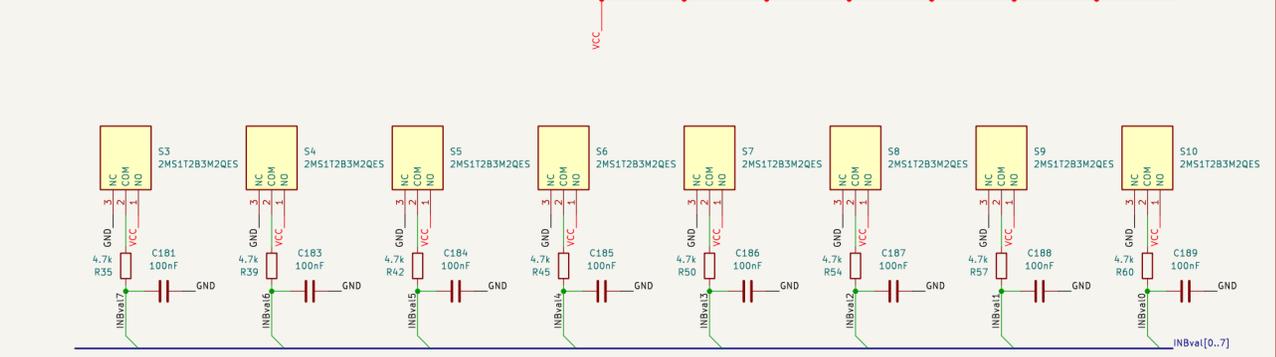
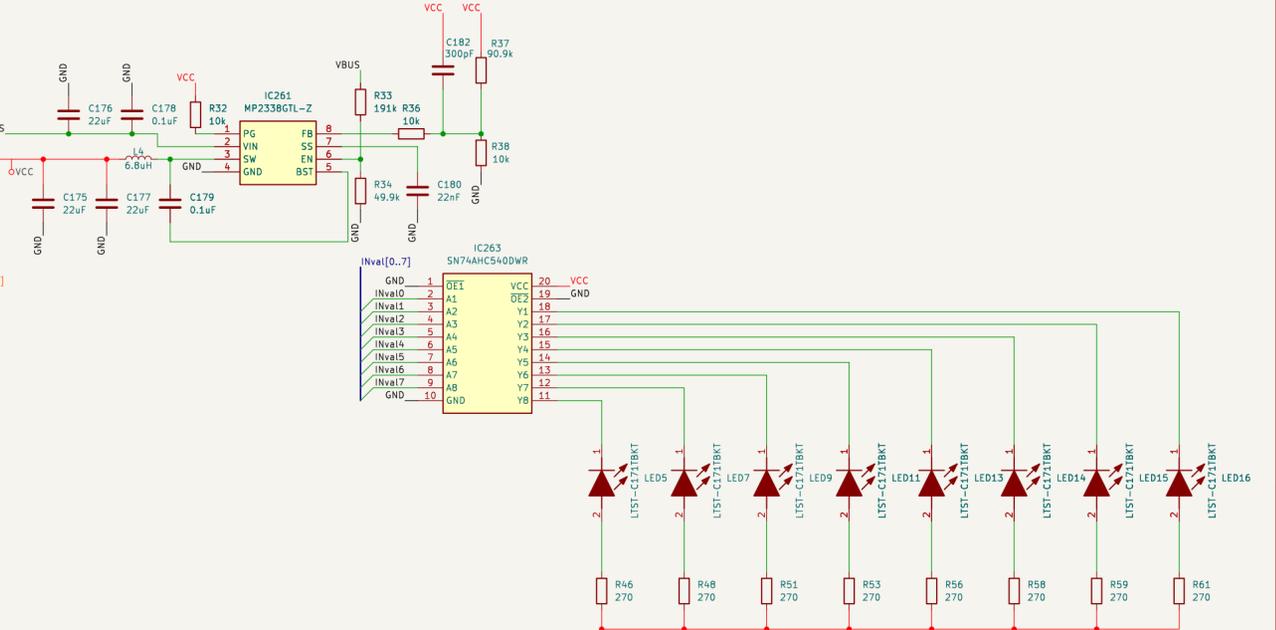
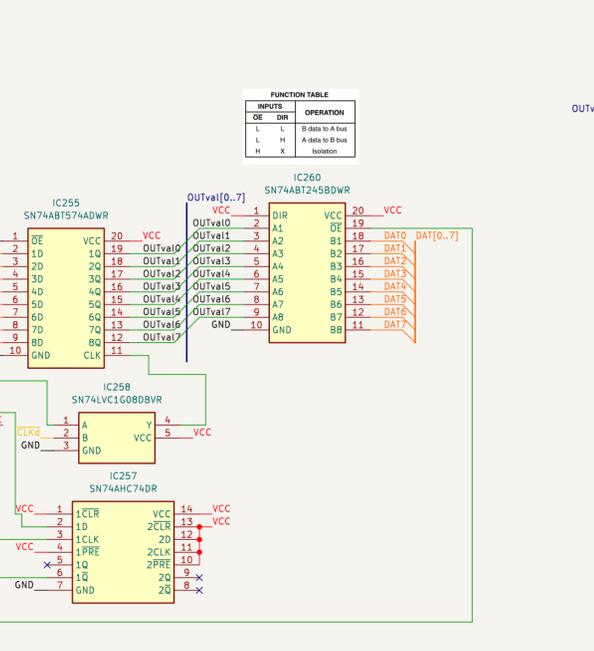
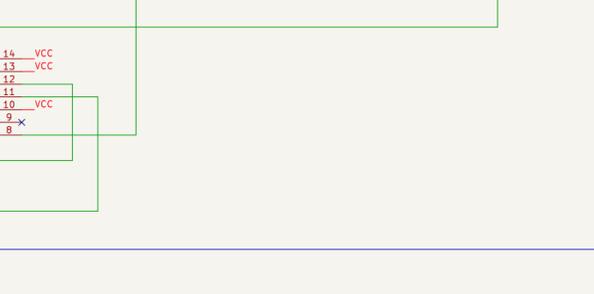
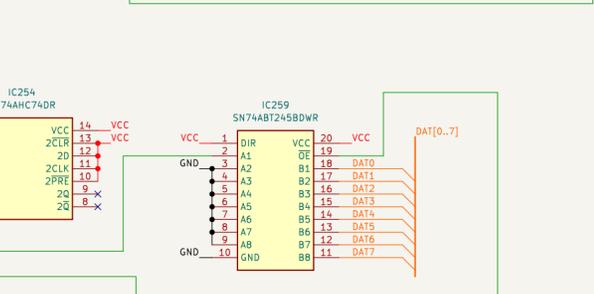
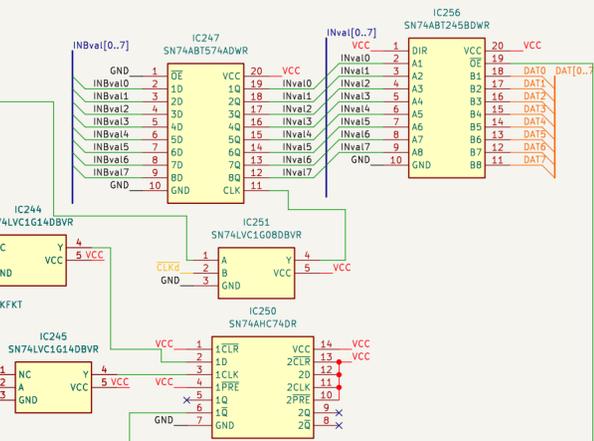








FUNCTION TABLE		
INPUTS	DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation



Switches