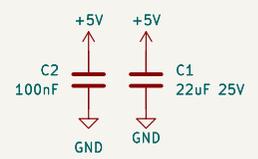
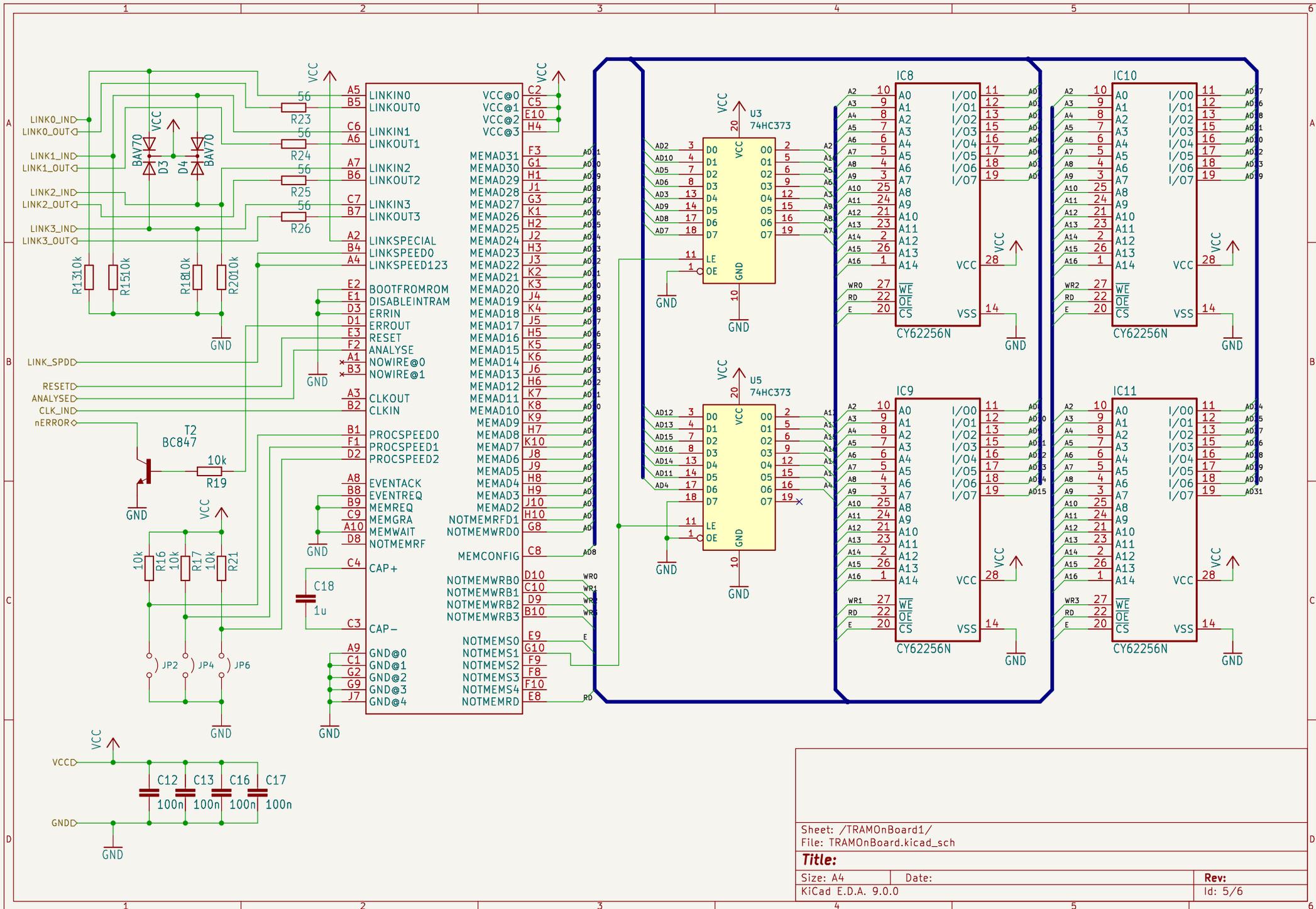


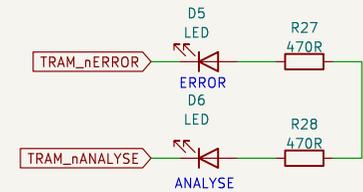
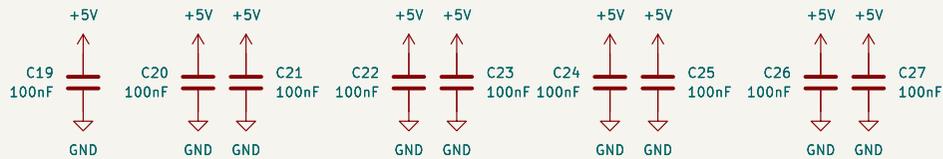
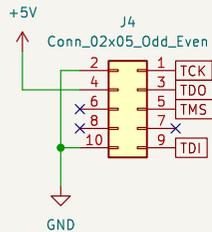
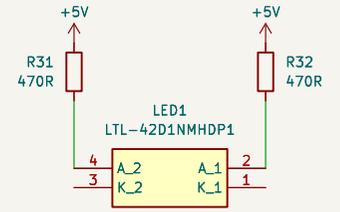
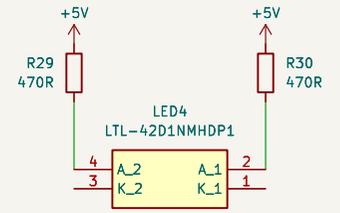
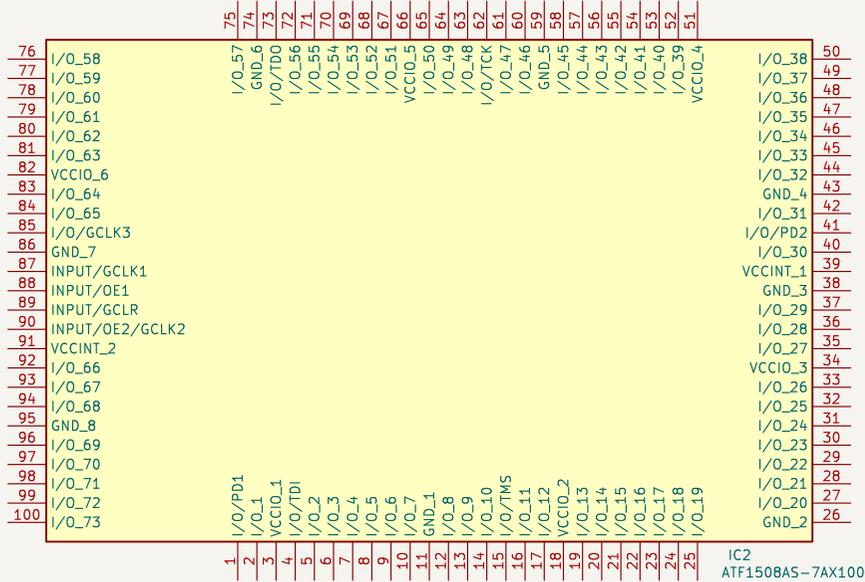
These are the CORRECT way around

Diodes for nSLOW0/nSLOW1/nRAMDISABLE and nROMDISABLE are on the main board so are not needed here. All ACTIVE LOW
 CPLD_nDIS has pull up main board, ACTIVE LOW



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