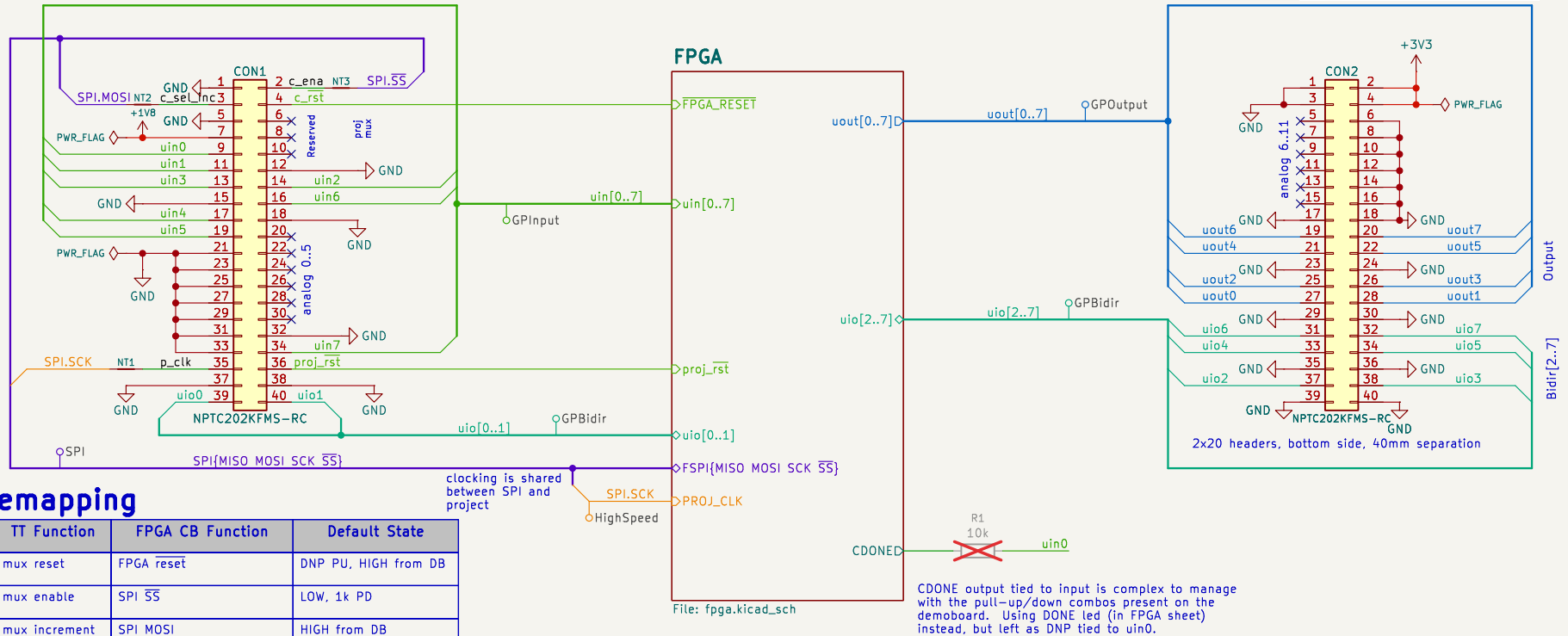
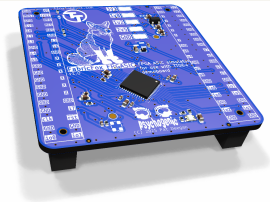




FabricFox FPGASIC

This is a minimalist FPGA board to be used as an "ASIC simulator" atop Tiny Tapeout demoboards (TT06+). The RP2 on the DB is charged with configuring the up5k FPGA, which is configured in CRAM mode, and awaits programming on power-up. The two (bottom side) connectors match the footprint of the ASIC breakout boards and map all the digital I/O, as well as project clock and reset, to the FPGA.



Pin Remapping

TT DB	TT Function	FPGA CB Function	Default State
c_rst	mux reset	FPGA reset	DNP PU, HIGH from DB
c_ena	mux enable	SPI SS	LOW, 1k PD
c_sel_inc	mux increment	SPI MOSI	HIGH from DB
proj_clk	project clock	SPI SCK + project clock	LOW from DB
ui_in0	ASIC in0	CDONE output	Done state, through 1k

To program using CRAM, we need independent control of:

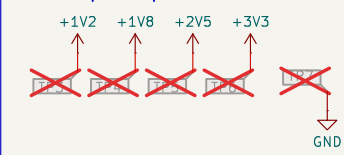
- * FPGA RESET
- * SPI
 - CLOCK
 - MOSI and
 - SS

So 4 pins. We have 3 from the project MUX but we can dual-purpose the project clock as a SPI clock.

For detection, the demoboards pull up c_ena (CON1 pin 2) and creset (CON1 pin 4) with a 10k. TT06 carrier pulls both these down strongly (1k), whereas they stay high for TT04/disconnected. To detect FPGA, pull "one" of these down, leave the other high.

Since FPGA SS needs to default to LOW to go into CRAM mode by default, this should then be on ena or reset. c_ena makes most logical sense (when sending SPI data, it is low, otherwise... enabled), and that way creset is reframed as FPGA reset, which also makes sense.

5019 Testpoint clips

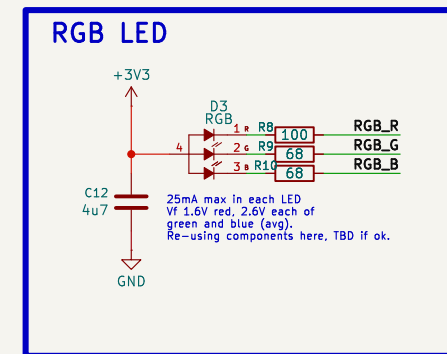
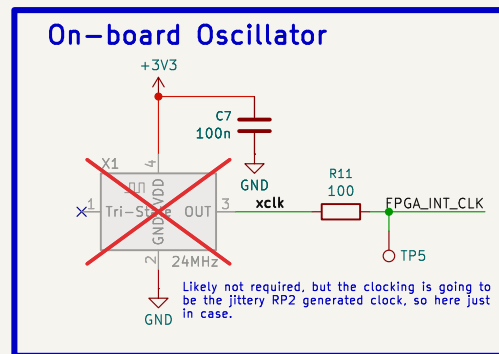
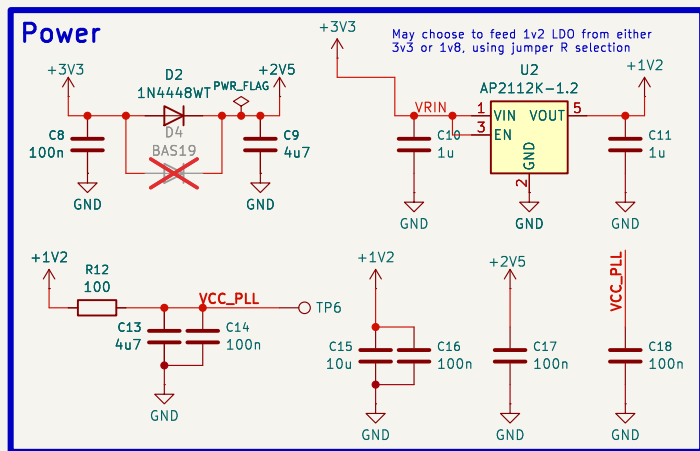
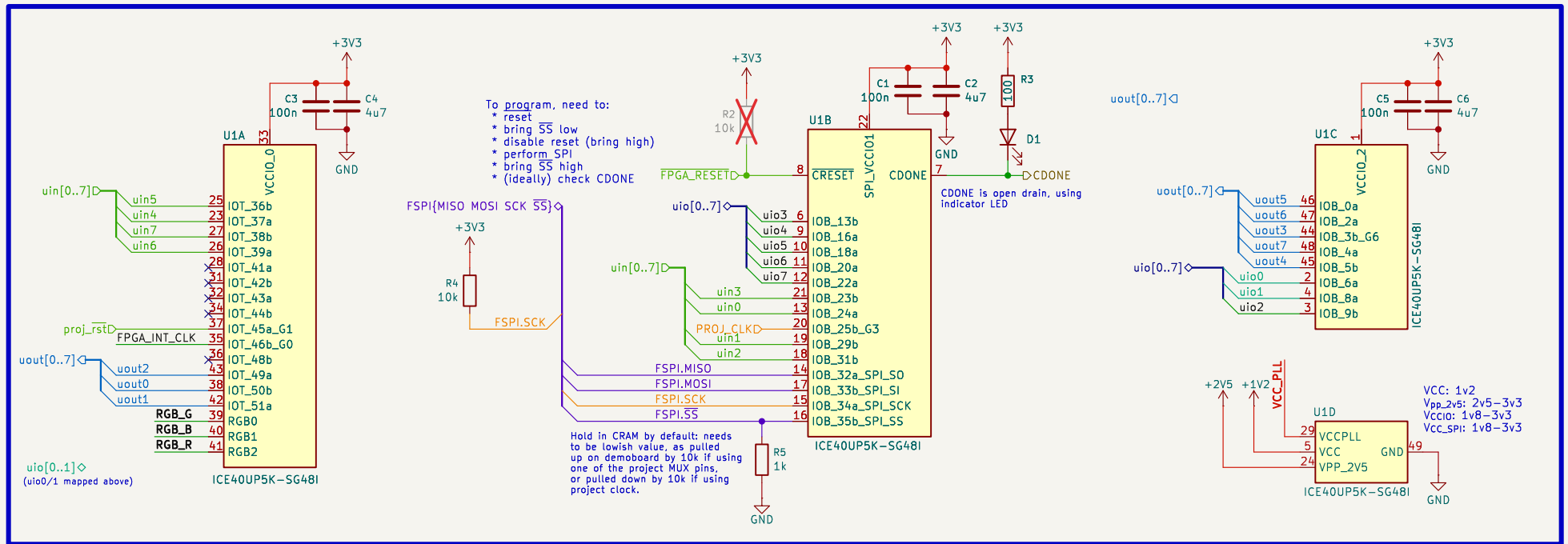


- FID1 Fiducial
- FID2 Fiducial
- FID3 Fiducial

Fox icon based on image by Stampf @ Pixabay.com

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Sheet: /
File: tt06-fpga-ICE40UP5k.kicad_sch
Title: FabricFox FPGASIC
Size: A4 Date: 2025-08-01 Rev: 1.1
KiCad E.D.A. 9.0.0 Id: 1/2

UP5K FPGA and Support



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Sheet: /FPGA/
File: fpga.kicad_sch

Title: UP5K FPGA and Support

Size: A4 Date: 2025-12-01

KiCad E.D.A. 9.0.0

Rev: 1.0

Id: 2/2