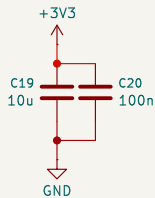
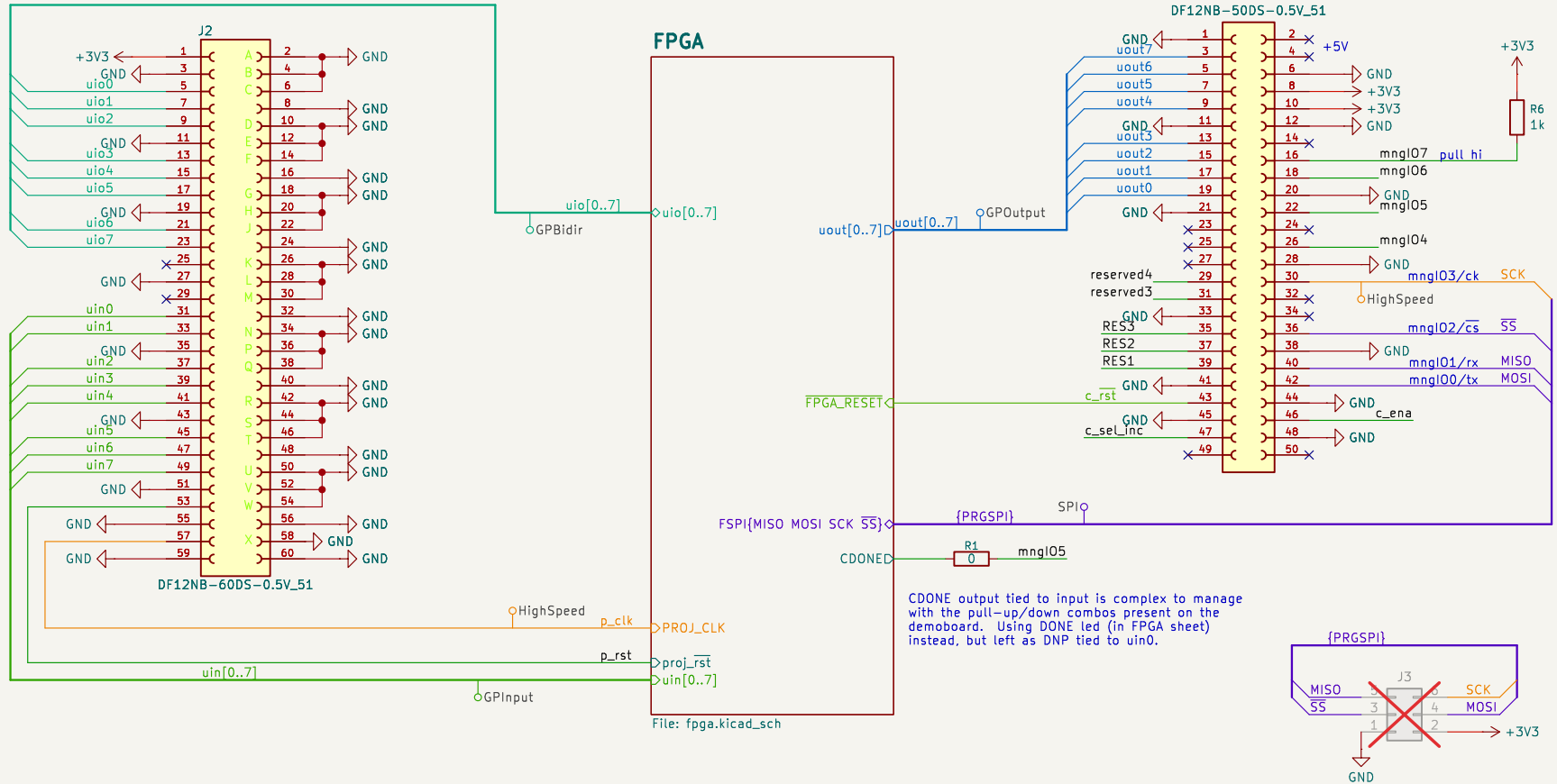
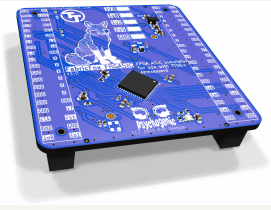




FabricFox FPGASIC

This is a minimalist FPGA board to be used as an "ASIC simulator" atop Tiny Tapeout demoboard (TT06+). The RP2 on the DB is charged with configuring the up5k FPGA, which is configured in CRAM mode, and awaits programming on power-up. The two (bottom side) connectors match the footprint of the ASIC breakout boards and map all the digital I/O, as well as project clock and reset, to the FPGA.

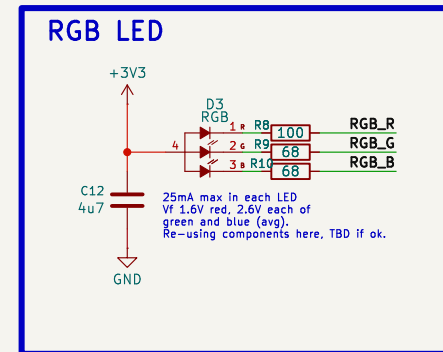
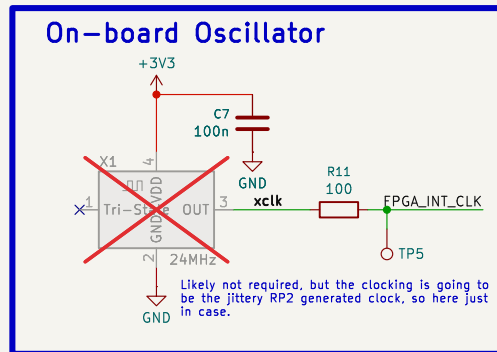
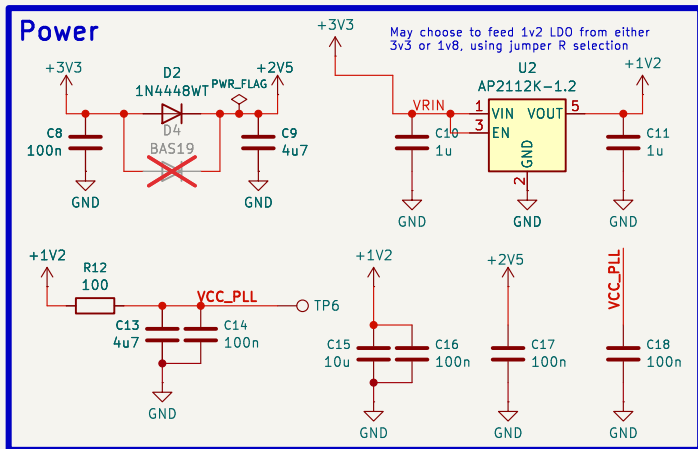
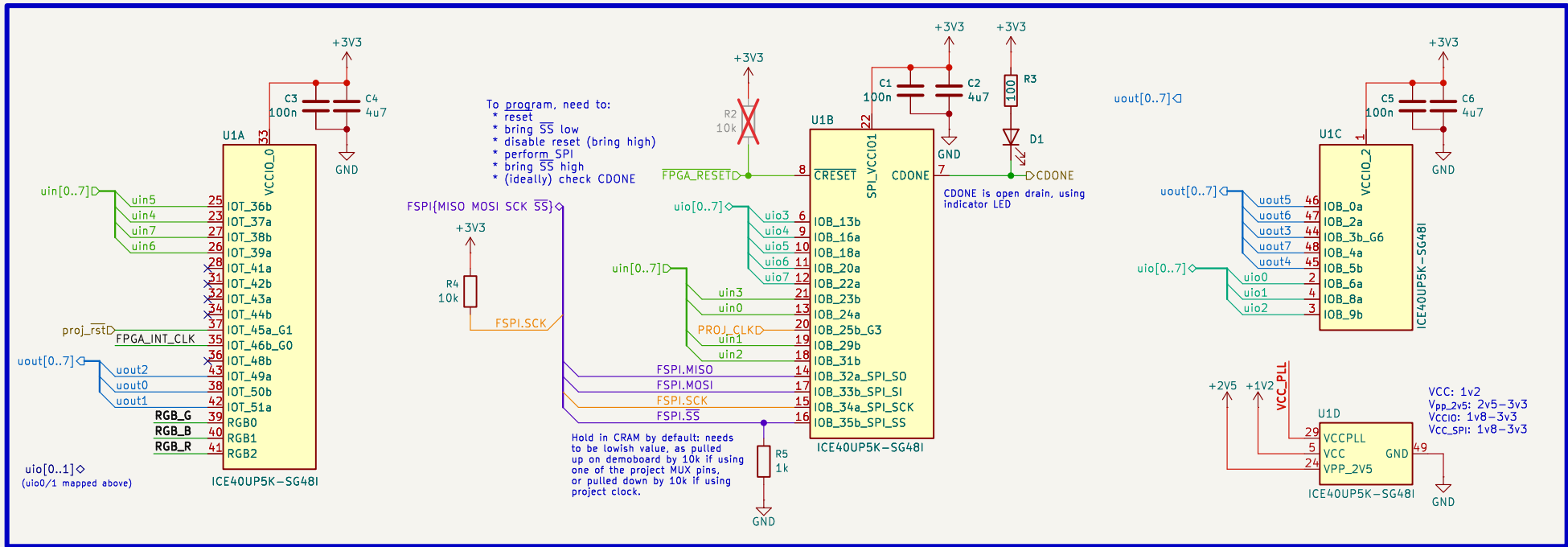


- FID1 Fiducial
- FID2 Fiducial
- FID3 Fiducial

Fox icon based on image by Stampf @ Pixabay.com

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Psychogenic Technologies INC
Sheet: /
File: ttdebv3-fpga-ICE40UP5k.kicad_sch
Title: FabricFox FPGASIC
Size: A4 Date: 2025-12-01 Rev: 2.0
KiCad E.D.A. 9.0.0 Id: 1/2

UP5K FPGA and Support



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Psychogenic Technologies INC

Sheet: /FPGA/
File: fpga.kicad_sch

Title: UP5K FPGA and Support

Size: A4	Date: 2025-12-01
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KiCad E.D.A. 9.0.0

Rev: 1.0

Id: 2/2