

soc_power



File: 09.kicad_sch

soc_power_decaps



File: 10.kicad_sch

soc_power_vss



File: 11.kicad_sch

ddr



File: 12.kicad_sch

mmc



File: 13.kicad_sch

ospi



File: 14.kicad_sch

temp_id_detect



File: 15.kicad_sch

cpsw3g_rmii_phy



File: 16.kicad_sch

boot_mode



File: 20.kicad_sch

current_mon



File: 21.kicad_sch

jtag



File: 23.kicad_sch

usb2



File: 25.kicad_sch

prg0_prg1



File: 27.kicad_sch

gpmc



File: 28.kicad_sch

display_spi_can



File: 29.kicad_sch

pcie



File: 30.kicad_sch

eth_pcie_clock



File: 31.kicad_sch

eth_led_adc



File: 32.kicad_sch

io_expander



File: 33.kicad_sch

mcu_general



File: 34.kicad_sch

reset



File: 35.kicad_sch

main_power



File: 36.kicad_sch

3V3_5V



File: 37.kicad_sch

soc_power_supply



File: 38.kicad_sch

peripheral_power_supply



File: 39.kicad_sch

fixpcb



File: fixpcb.kicad_sch

usb-power-efuse



File: usb-power-efuse.kicad_sch

Sheet: /
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Title:

Size: A4

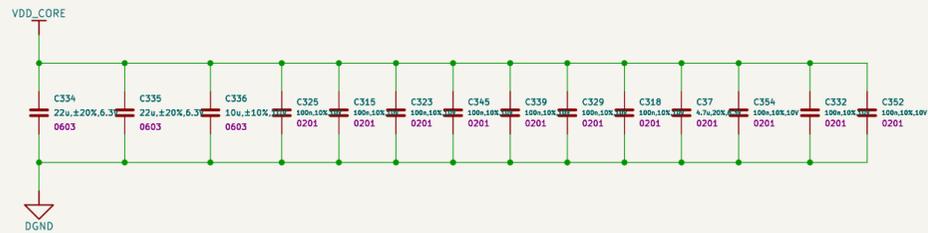
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KiCad E.D.A. 9.0.0

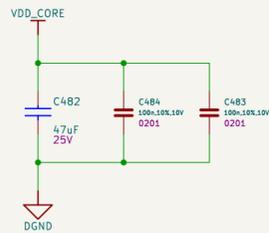
Rev:

Id: 1/28

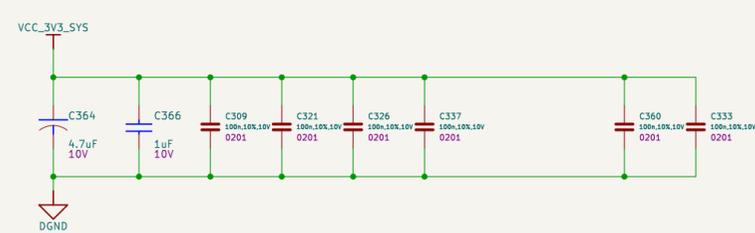
SOC POWER SUPPLIES – DECAPS



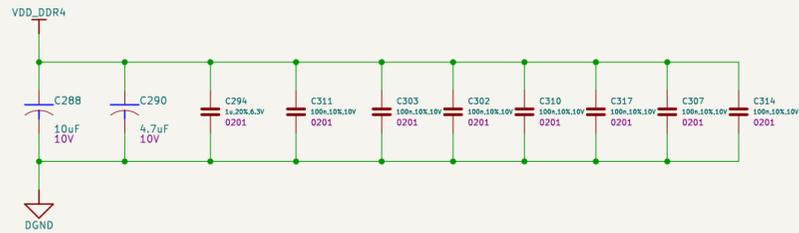
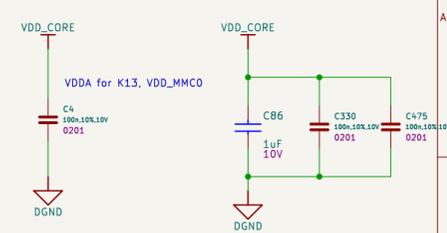
Cad Note :- Place 0.1 uF caps near to SoC pins



Cad Note :- To place after current sense resistor on VDD_CORE plane



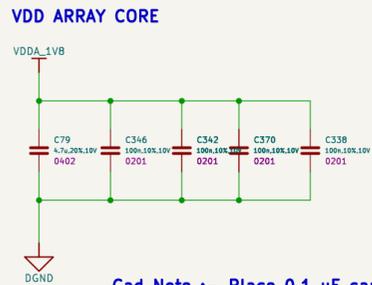
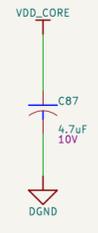
Cad Note :- Place 0.1 uF caps near to SoC pins



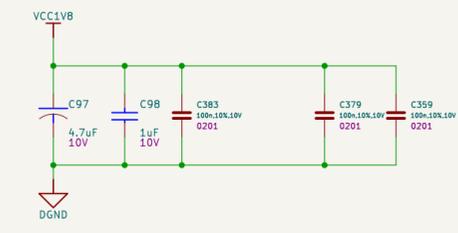
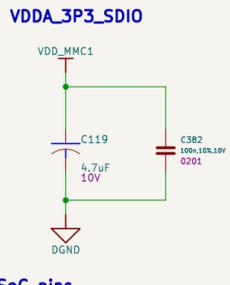
Cad Note :- Place 0.1 uF caps near to SoC pins



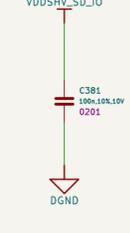
Cad Note :- Place 0.1 uF caps near to SoC pins



Cad Note :- Place 0.1 uF caps near to SoC pins



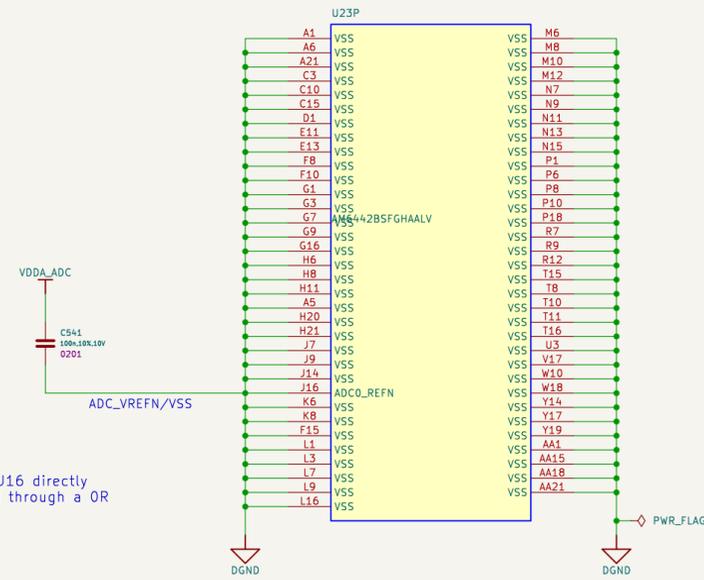
Cad Note :- Place 0.1 uF caps near to SoC pins



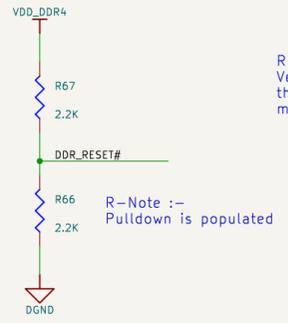
SoC POWER – VSS

CAD Note:
Place CAP C541
between pins
J15 and J16

D-Note :-
ADCO_REFN
Connect the decap to J16 directly
Connect J16 to ground through a 0R



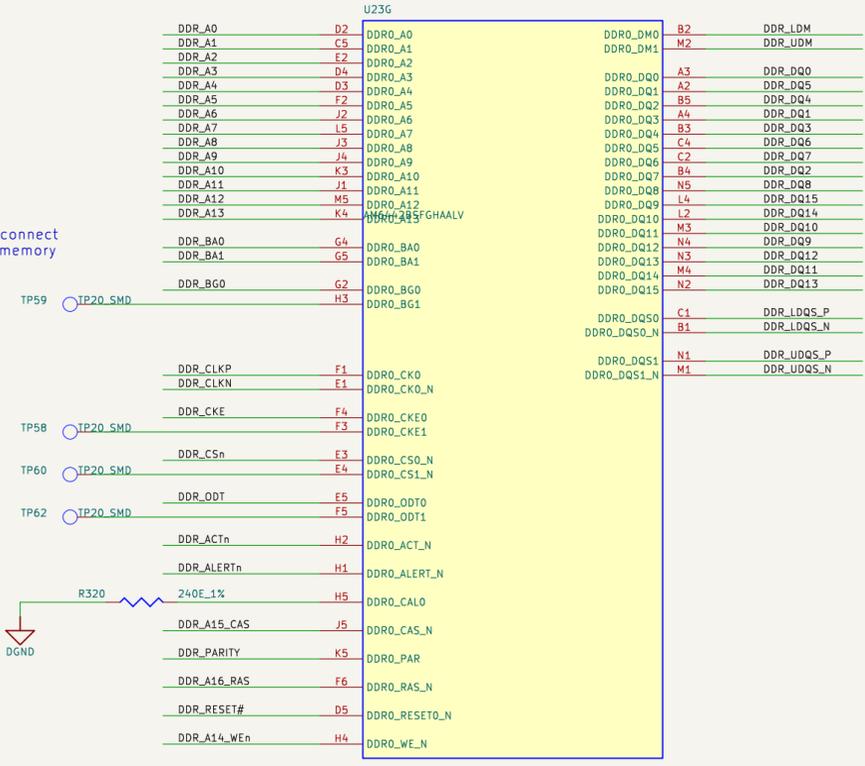
SoC DDR INTERFACE



R-Note :-
Verify need to connect
DDR0_BG1 for memory
expansion

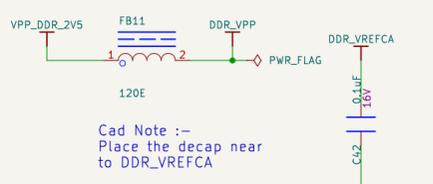
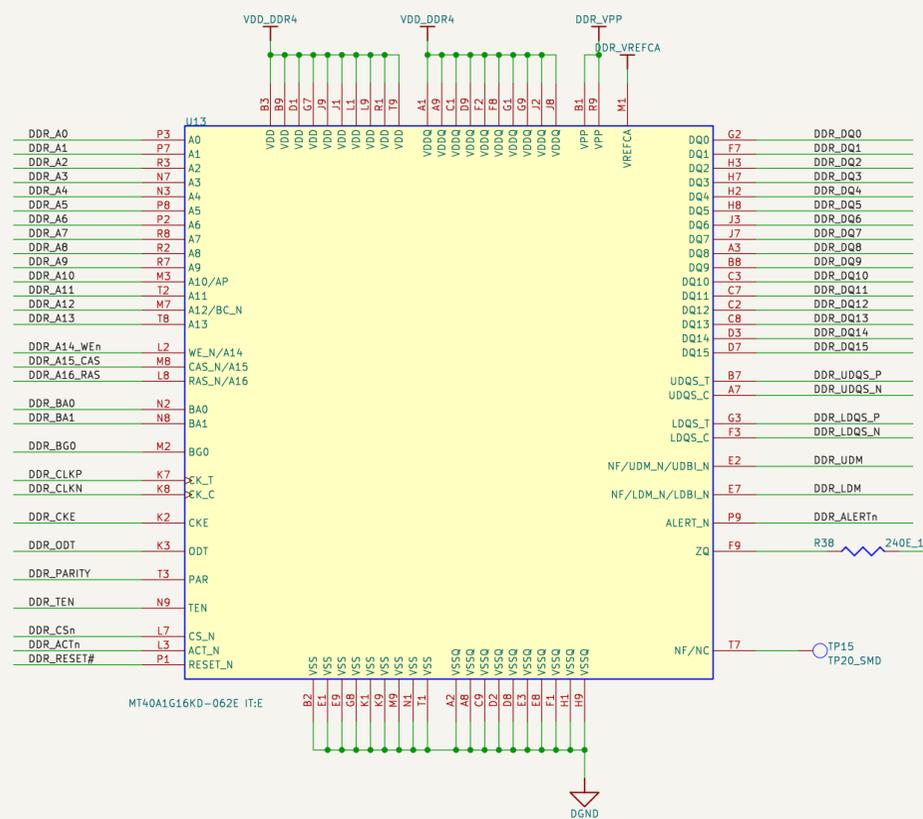
R-Note :-
Verify need to connect
these NC pins for
memory expansion

R-Note :-
Pulldown is populated

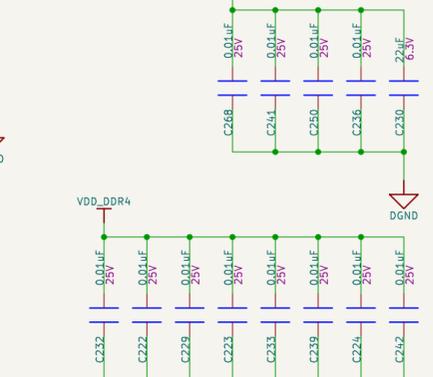
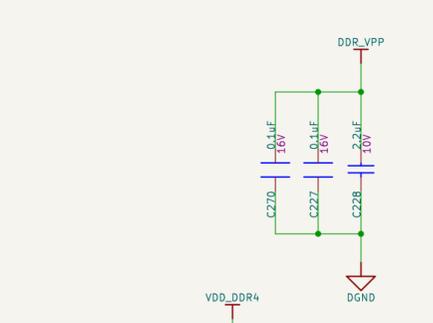


D-Note :-
DDR DQ Lines Swapped
With Data Byte

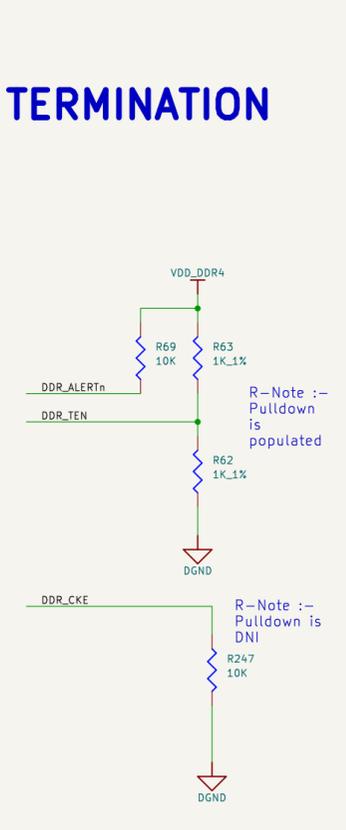
DDR4 DEVICE



Cad Note :-
Place the decap near
to DDR_VREFCA

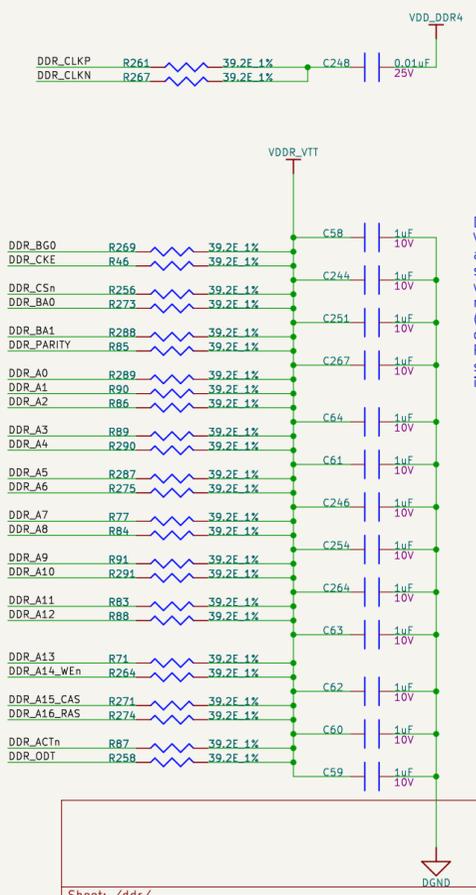


DDR TERMINATION



R-Note :-
Pulldown is
populated

R-Note :-
Pulldown is
DNI



D-Note:-
VTT terminations for
address and control
signals is optional
when a single DDR4
memory is used
(Point-Point)
connection
Refer SK-AM62B-P1
schematics for
implementation

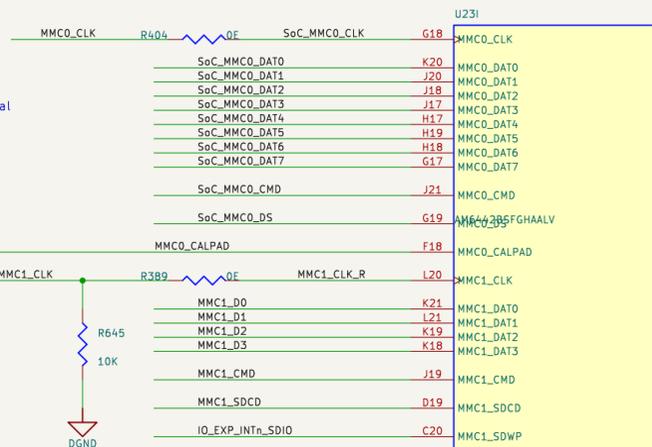
D-Note :-
This family of processor implements a hard and dedicated PHY for eMMC interface.
The pull required for D0..D7, Clock and other eMMC interface control signals are enabled internal to the SOC during reset
Refer pin connectivity table for guidelines when eMMC is not used

D-Note :-
The pulls required for D0..D7, Clock and other eMMC interface control signals are enabled internal to the SOC during reset and are eMMC JEDEC standard compliant
External pullup is optional and can be deleted on the custom board
Refer pin connectivity table for guidelines when eMMC is not used

eMMC FLASH

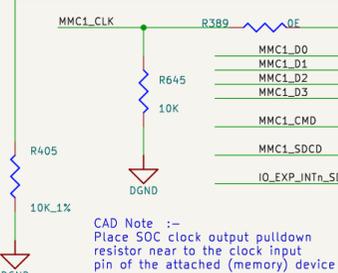
D-Note :-
OE provision on MMC0_CLK
Helps improve signal integrity

SOC - MMC INTERFACE



D-Note :-
MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51)

R-Note :-
What is the reason we selected pullup for MMC - SD card or other peripherals?
Because there are cases where the clock is stopped or paused in a low logic state and the pull-down option is consistent with this logic state.

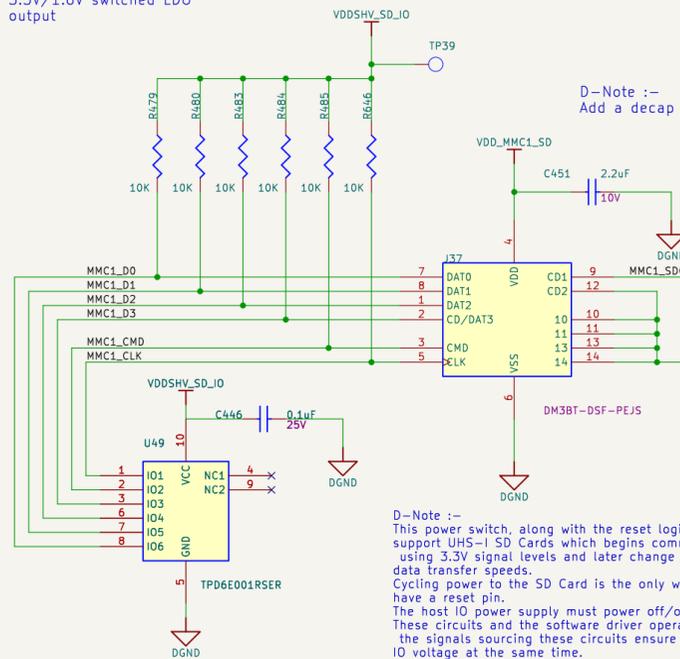


D-Note :-
The GPIO reset option makes it possible for software to reset the attached device (eMMC or OSPI or SD card or OLDIO or EPHY) without resetting the entire processor if there is a case where the peripheral becomes unresponsive.

D-Note :-
You could eliminate the GPIO option and only use the reset output (Warm or Cold), where software forces a warm reset if the peripheral becomes unresponsive. However, this will reset the entire device rather than trying to recover the specific peripheral without resetting the entire device.

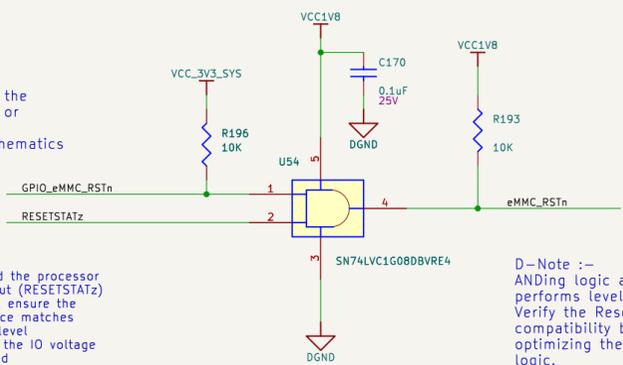
D-Note :-
For UHS-I operation, the pullups are recommended to be connected to the 3.3V/1.8V switched LDO output

D-Note :-
Ensure internal pullups are not configured when 10K external pullups are used. As a good design practice, a 47K pullup is recommended to ensure the pullup value is within the SD card specification, when internal pullups are enabled unexpectedly. This way the resulting pull resistance will still be within the specified.



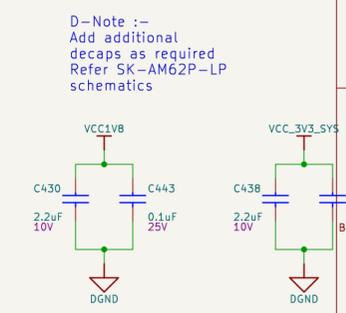
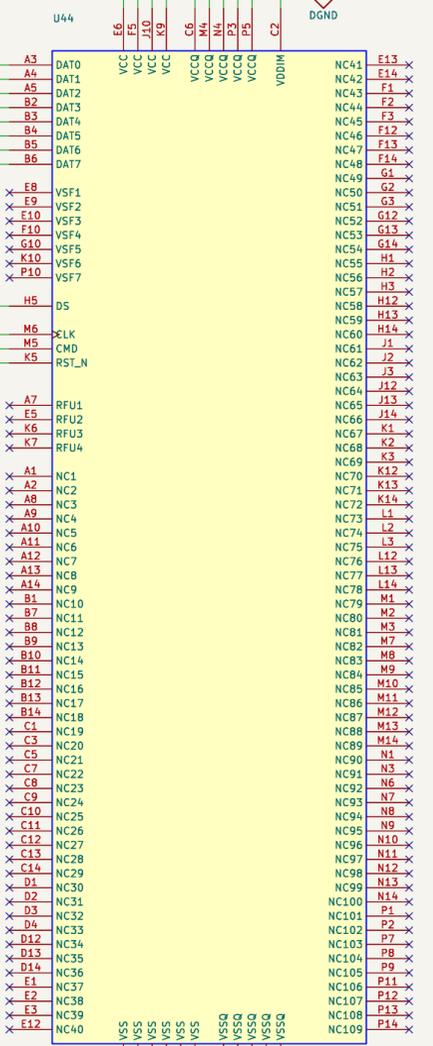
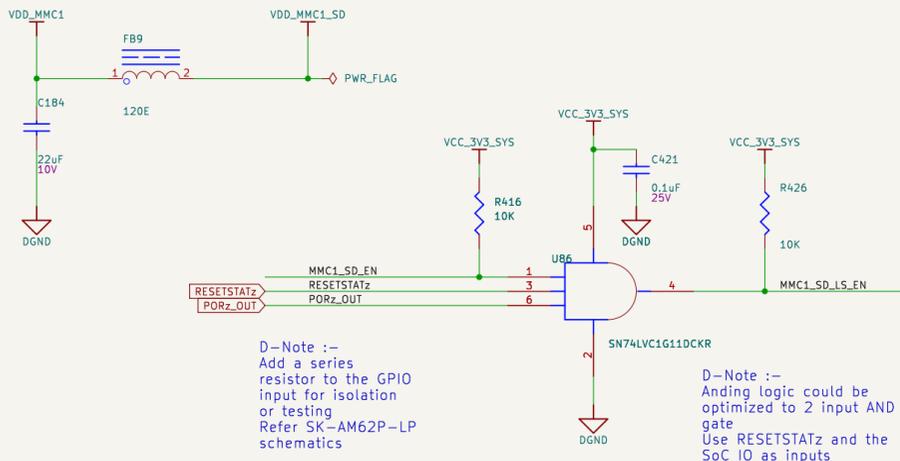
D-Note :-
Add a series resistor to the GPIO input for isolation or testing
Refer SK-AM62P-LP schematics

eMMC FLASH RESET



D-Note :-
In case ANDING logic is not used and the processor Main Domain warm reset status output (RESETSTATz) is used to reset the attached device, ensure the IO voltage level of the attached device matches the RESETSTATz IO voltage level. A level translator is recommended to match the IO voltage level. A resistor divider could be used alternatively, provided optimum impedance value of the resistor divider is selected. If too high the rise/fall time of the eMMC reset input could be slow and introduce too much delay. If too low it will cause the AM62x to source too much steady-state current during normal operation.

SD CARD INTERFACE

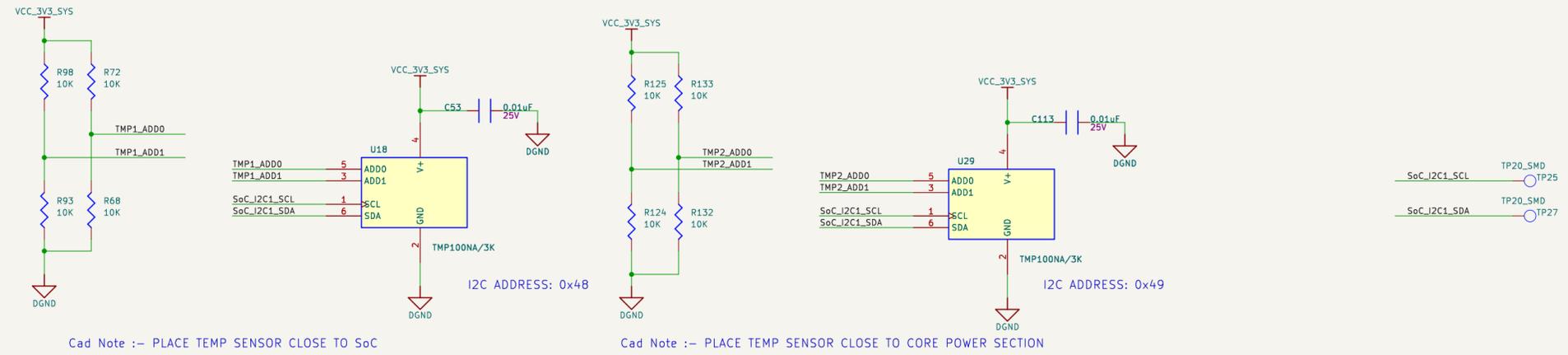


From & To IO Expander

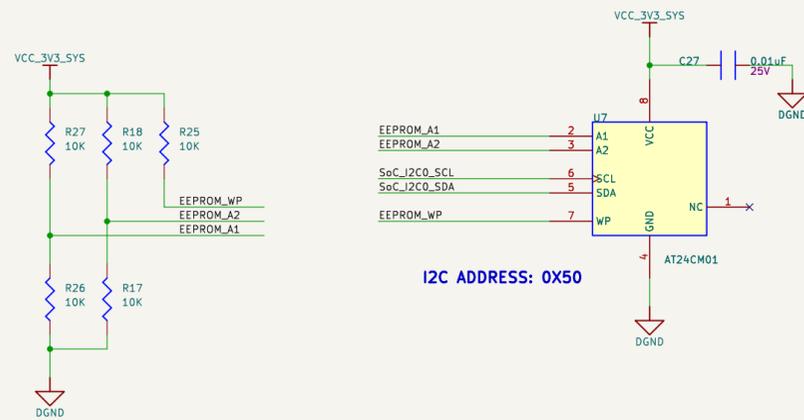
IO_EXP_INTn_SDIO	IO_EXP_INTn_SDIO
GPIO_eMMC_RSTn	GPIO_eMMC_RSTn
MMC1_SD_EN	MMC1_SD_EN

Sheet: /mmc/
File: 13.kicad_sch
Title:
Size: User Date:
Kicad E.D.A. 9.0.0 Id: 7/28 Rev:

DIGITAL TEMPERATURE SENSOR

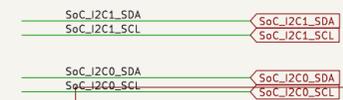


BOARD ID EEPROM



BOARD PRESENCE DETECT CIRCUIT

Off Page Connections



Sheet: /temp_id_detect/
File: 15.kicad_sch

Title:

Size: User Date: Rev:
KiCad E.D.A. 9.0.0

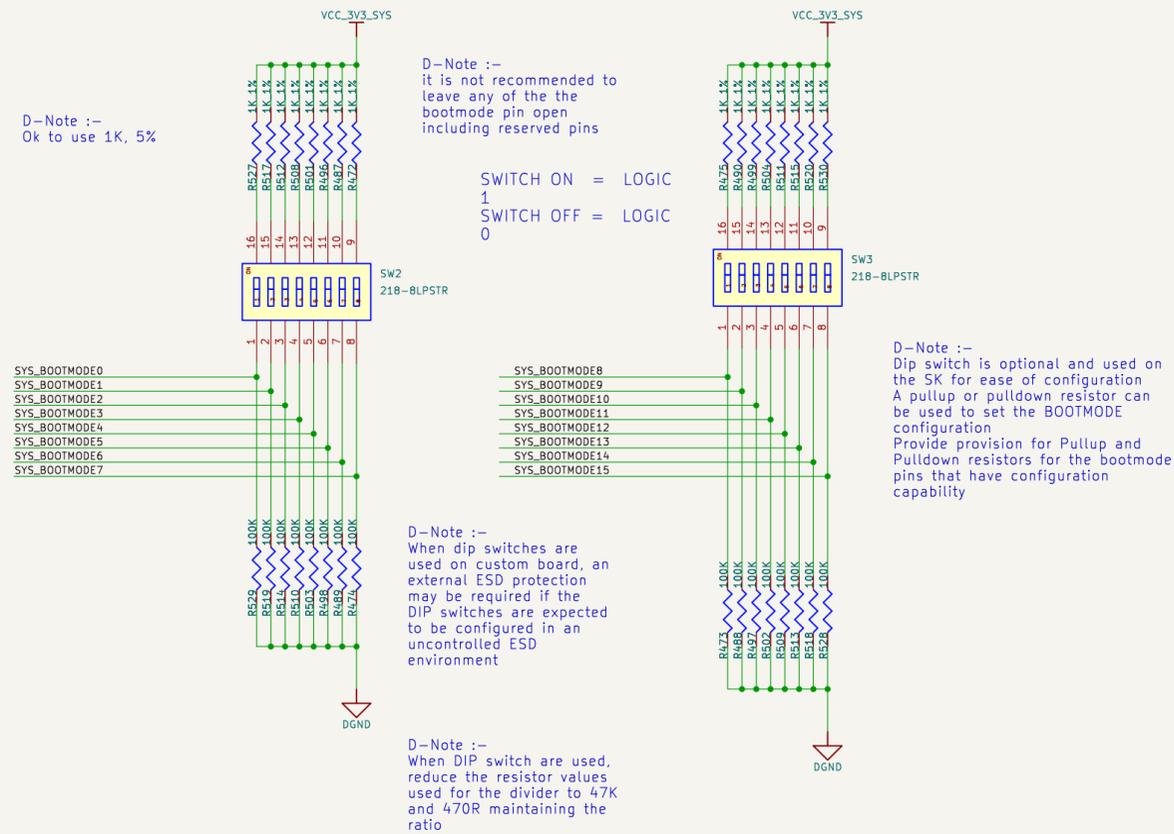
Id: 9/28

BOOT MODE BUFFER & DIP SWITCHES

SYS_BOOTMODE0	R325	1K 1%	BOOTMODE0
SYS_BOOTMODE1	R326	1K 1%	BOOTMODE1
SYS_BOOTMODE2	R327	1K 1%	BOOTMODE2
SYS_BOOTMODE3	R328	1K 1%	BOOTMODE3
SYS_BOOTMODE4	R329	1K 1%	BOOTMODE4
SYS_BOOTMODE5	R330	1K 1%	BOOTMODE5
SYS_BOOTMODE6	R331	1K 1%	BOOTMODE6
SYS_BOOTMODE7	R332	1K 1%	BOOTMODE7

SYS_BOOTMODE8	R372	1K 1%	BOOTMODE8
SYS_BOOTMODE9	R373	1K 1%	BOOTMODE9
SYS_BOOTMODE10	R374	1K 1%	BOOTMODE10
SYS_BOOTMODE11	R375	1K 1%	BOOTMODE11
SYS_BOOTMODE12	R376	1K 1%	BOOTMODE12
SYS_BOOTMODE13	R377	1K 1%	BOOTMODE13
SYS_BOOTMODE14	R378	1K 1%	BOOTMODE14
SYS_BOOTMODE15	R379	1K 1%	BOOTMODE15

BOOTMODE CONFIGURATION RESISTORS AND BOOTMODE SWITCHES

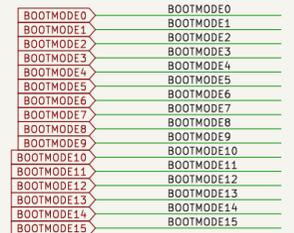


BOOT MODES SUPPORTED

1. OSPI
2. MMC1 – SD CARD
3. MMC0 – eMMC
4. CPSW Ethernet Slave
5. USB Host
6. USB Device
7. UART
8. Ethernet

Off Page Connections

From Processor

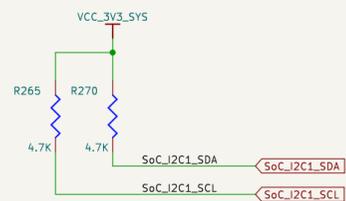


From Test Automation Header

CURRENT MONITORING DEVICES

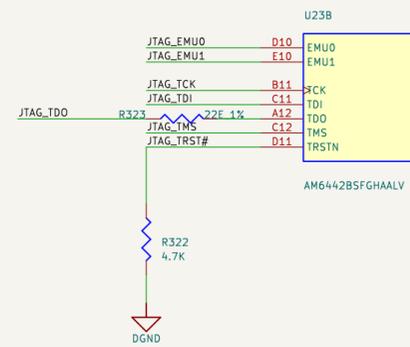
D-Note :-
 Note the supply rail name change across the shunt when optimizing the design (Deleting the current sense)

VDDA_1V8



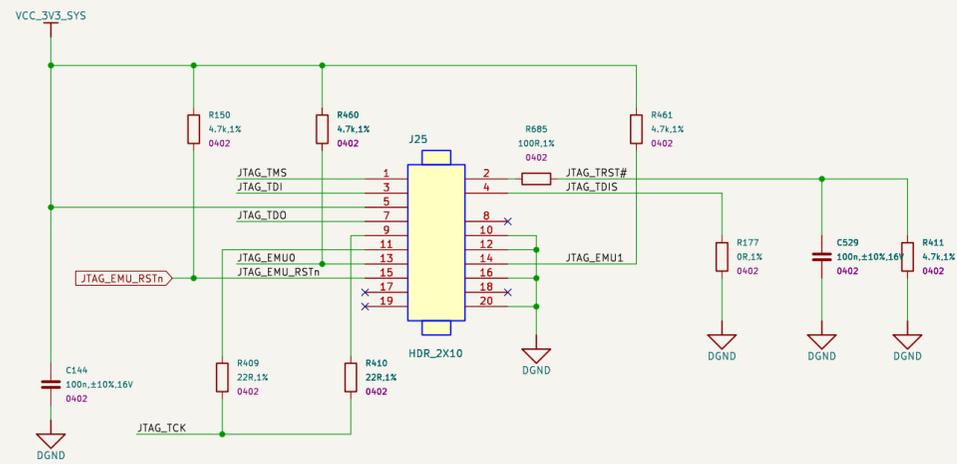
INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VDD_OV85	VDDAR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC1V8	SoC_DVDD1V8	4B
VDDA1V8	VDDA_1V8	4E
VCC1V2_DDR	VDD_DDR4	46

JTAG SoC SECTION



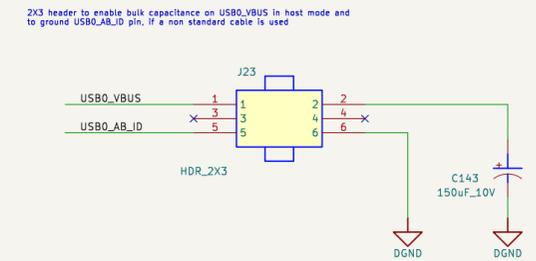
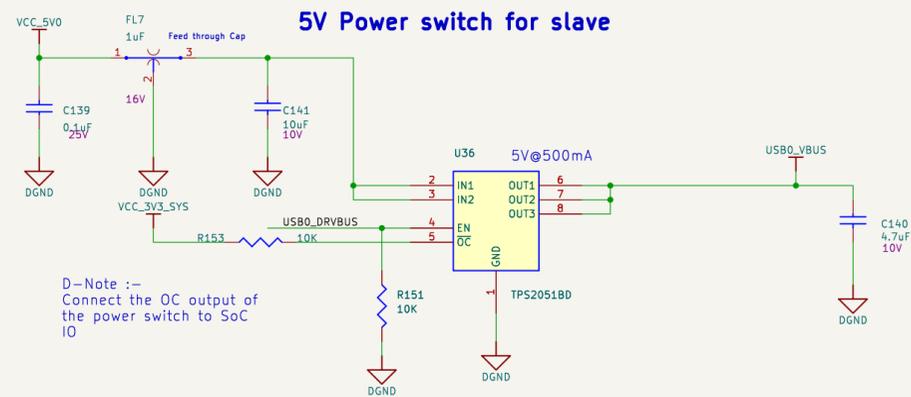
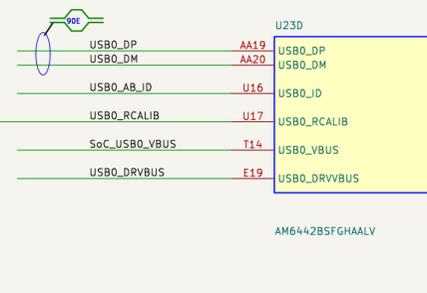
D-Note :-
Place pulls on JTAG signals near to the SoC
Refer AM62P schematics

JTAG 20 PIN cTI CONNECTOR

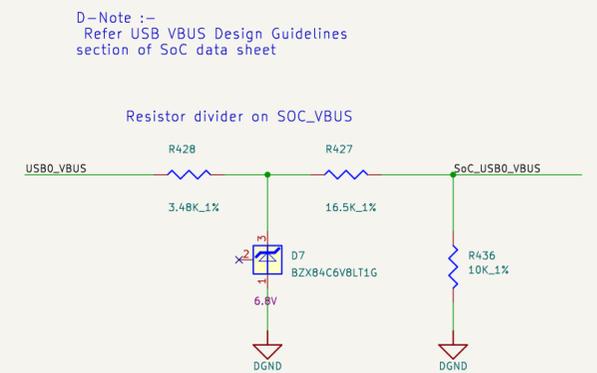
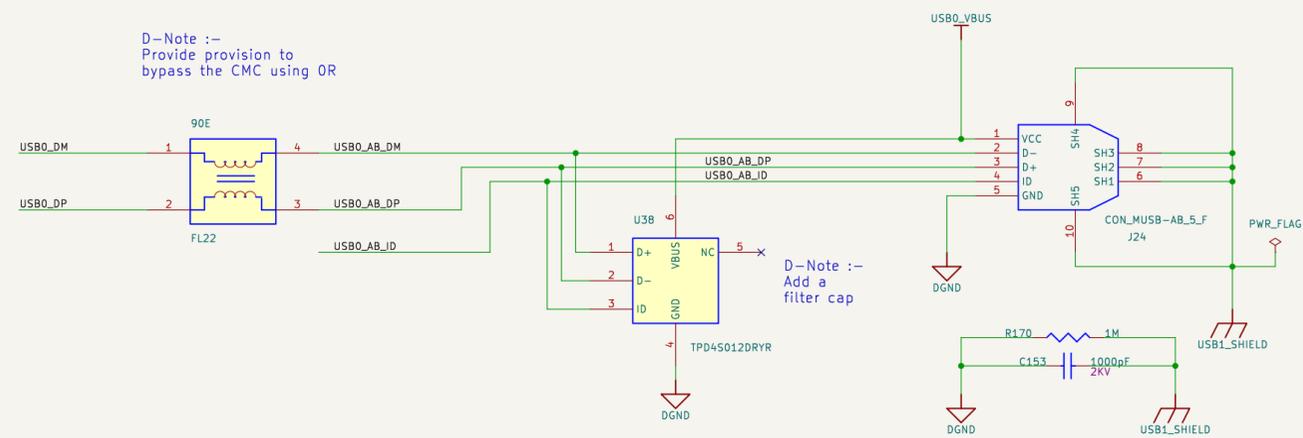


D-Note :-
TRSTn is the reset to the JTAG logic. For normal operation, this is pulled low, and thus the JTAG remains in reset as it is not being used. When a JTAG pod is connected, the pod will eventually drive this signal high to release the JTAG logic from reset and enable a JTAG connection.

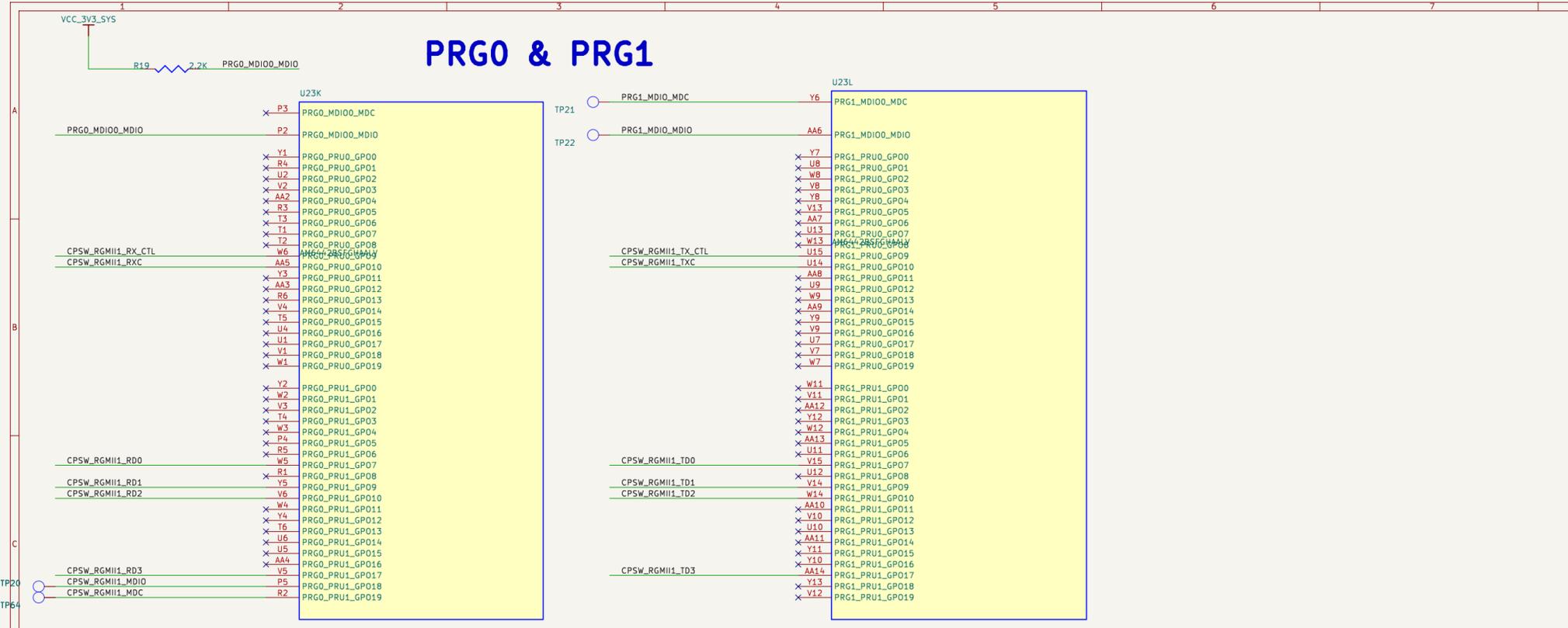
USB 2.0 INTERFACE



Micro USB 2.0 AB Connector



PRG0 & PRG1



D-Note :-
Add series resistors 22 R on the Ethernet interface TX (TDx) signals near to the SoC

HIGH SPEED EXPANSION CONNECTOR

To Presence Detect Buffer
From Processor GPMC

From FSI mux

From Processor GPMC resistor muxed with MIPI

From Processor

From clock Buffer

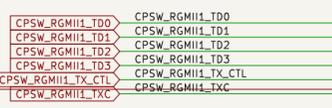
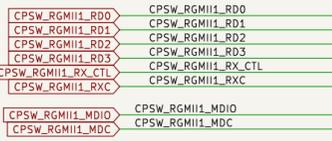
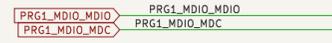
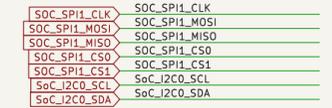
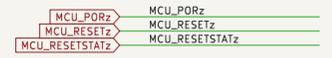
To and from ICSSG1 RGMII 2 Ethernet PHY

To and from ICSSG2 RGMII 1 Ethernet PHY

From MUX To HSE

To MUX From SoC

From CPSW RGMII 1 PHY



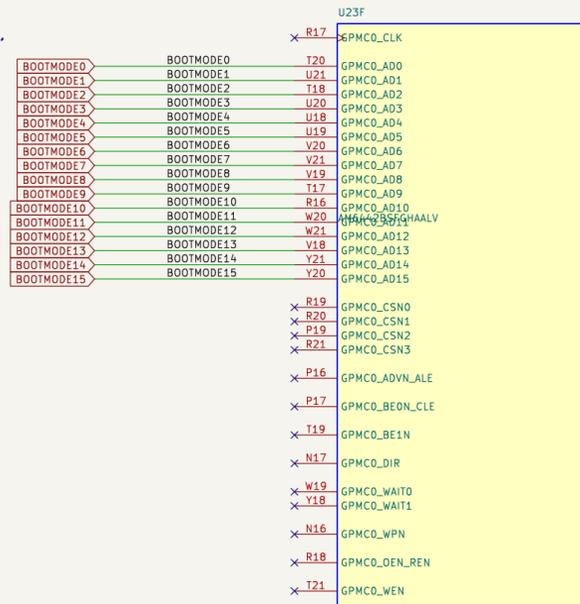
GPMC

D-Note :-
Add a series resistor OR
when used as GPMCO_CLK

D-Note :-
SOC IO buffers for signals used for GPMC
interface are disabled during reset
The required pulls for the interfaced
signals are provided on the GPMC interface
card

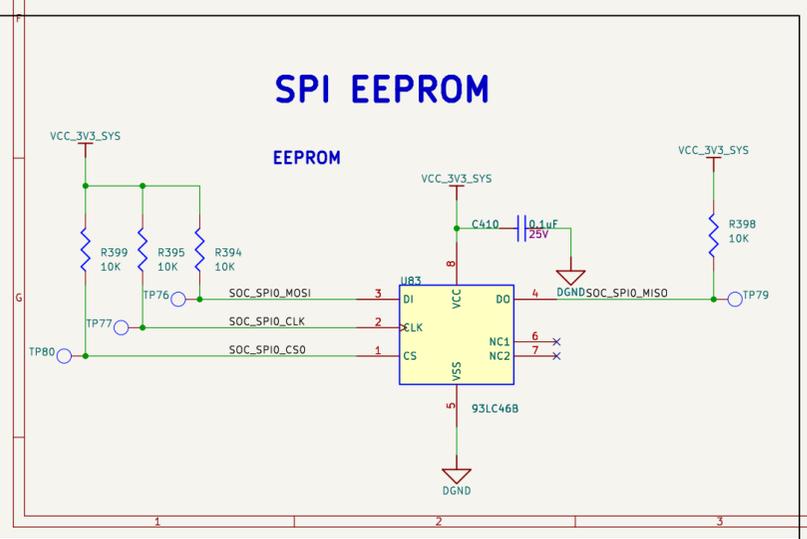
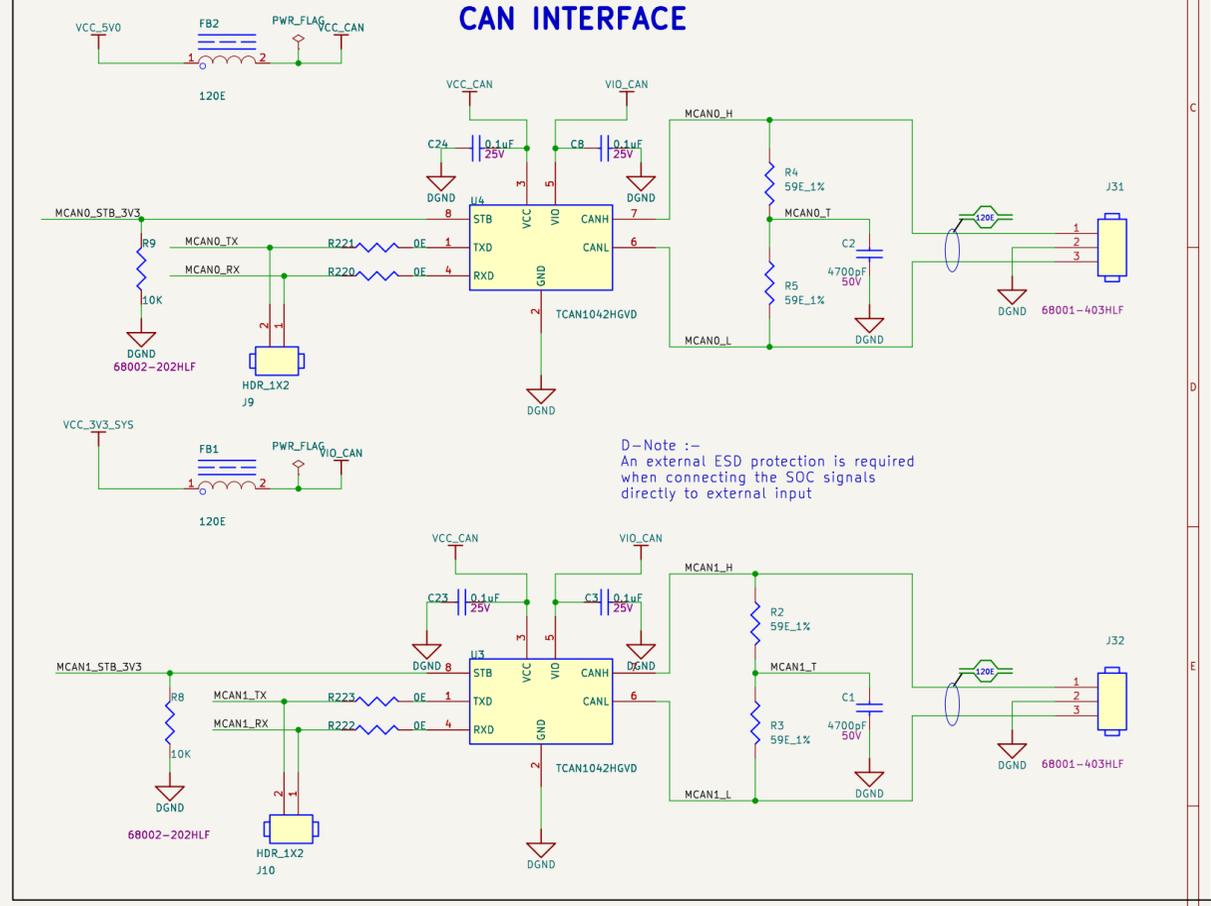
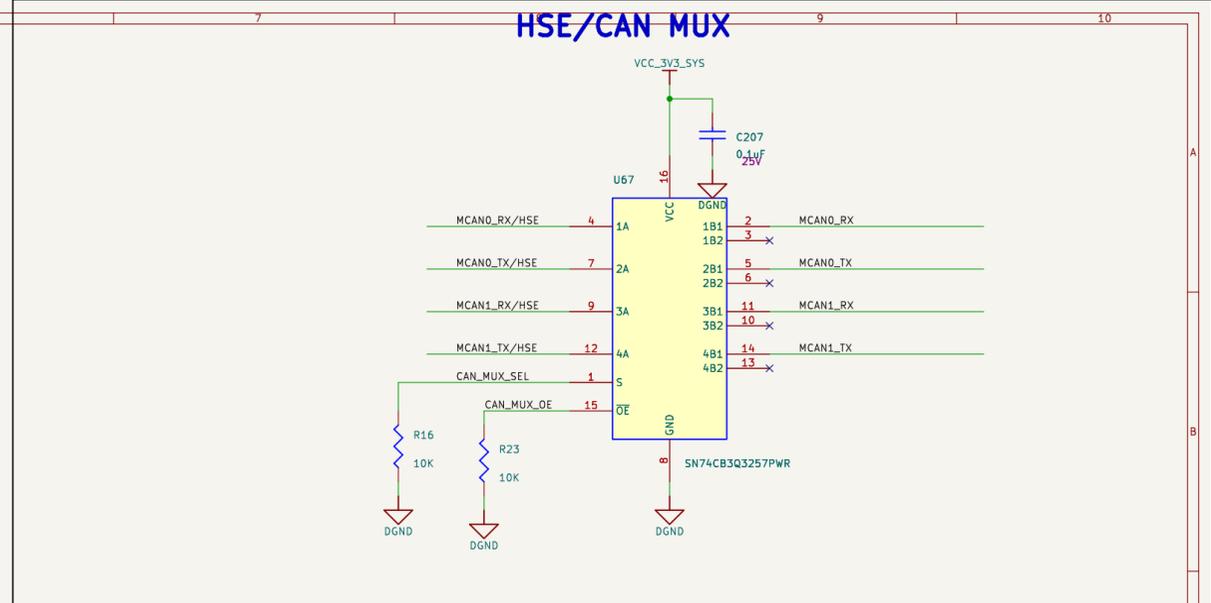
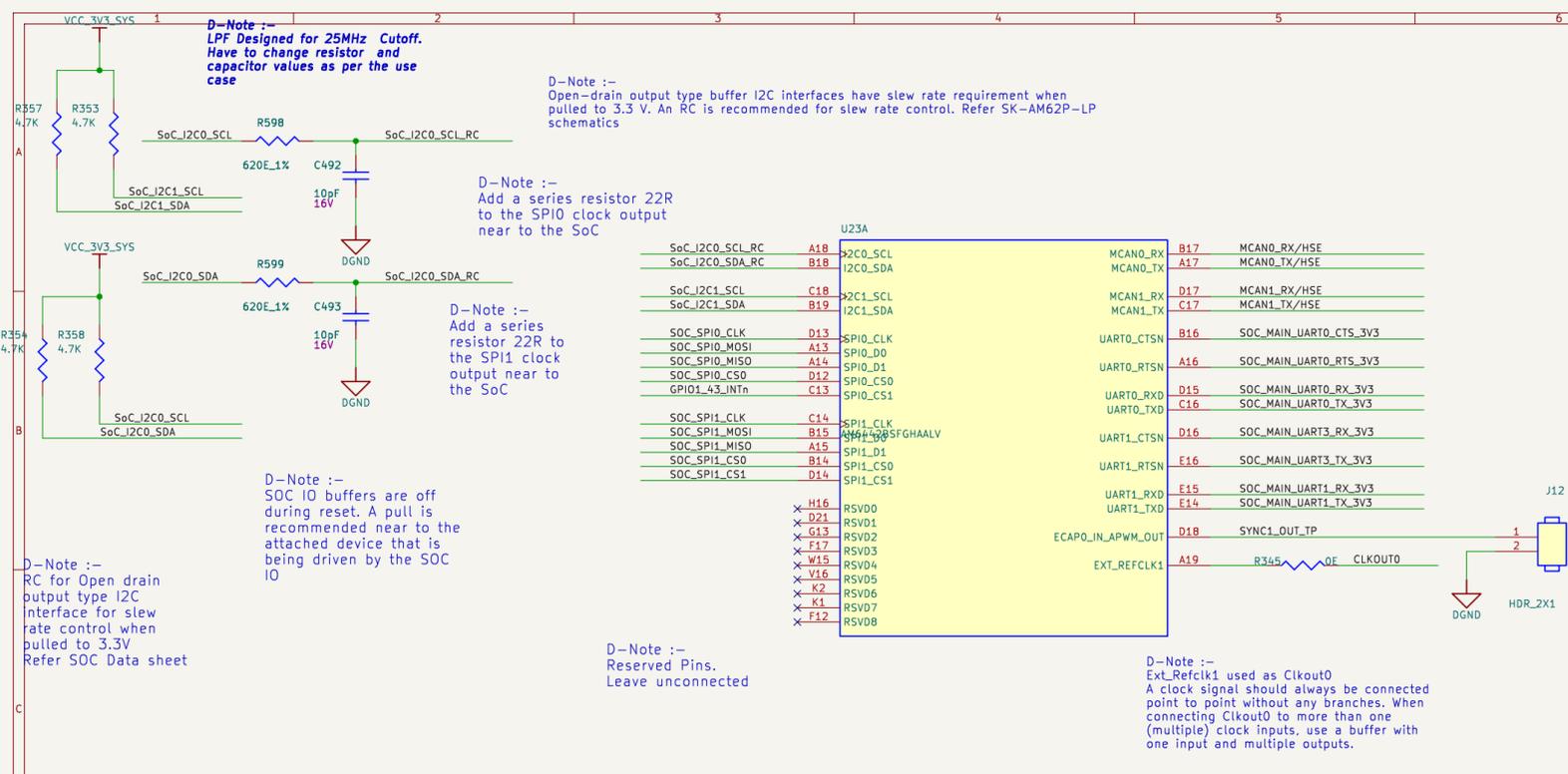
D-Note :-
Shorting of bootmode inputs (IOs) is
not recommended or allowed since the
IOs have alternate functions that could
be configured after boot
Shorting the bootmode pins directly to
VCC or ground directly is not
recommended
Connect each of the bootmode pins
through separate resistor
Choose the bootmode resistor value
based on the use case (10K or similar)

To Boot Mode Buffer .
HSE & MIPI Conn



TS3A27518ERTWR Truth Table

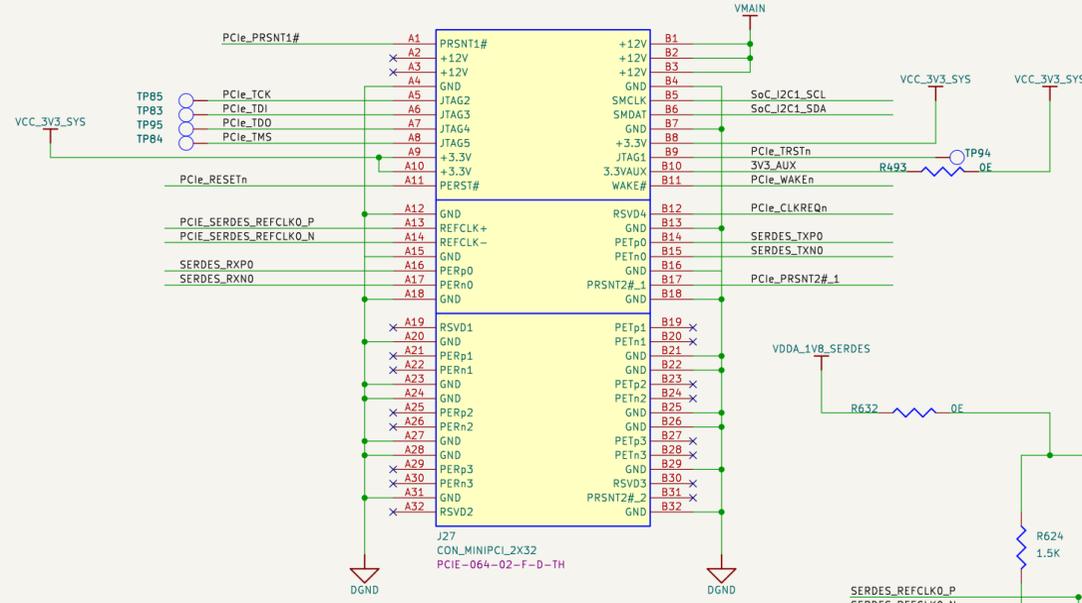
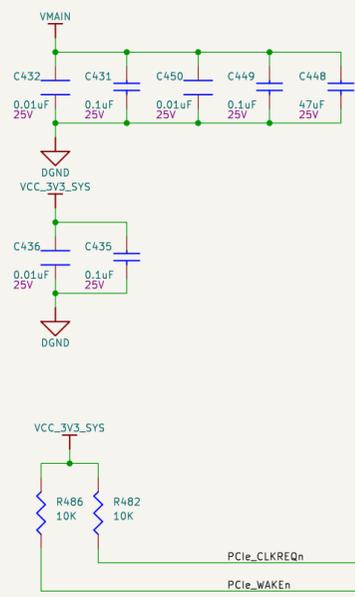
EN#	IN1	IN2	NC1/2/3 TO COM1/2/3 & COM1/2/3 TO NC1/2/3	NC4/5/6 TO COM14/5/6 & COM4/5/6 TO NC4/5/6	NO1/2/3 TO COM1/2/3 & COM1/2/3 TO NO1/2/3	NO4/5/6 TO COM14/5/6 & COM4/5/6 TO NO4/5/6
H	X	X	OFF	OFF	OFF	OFF
L	L	L	ON	ON	OFF	OFF
L	H	L	OFF	ON	ON	OFF
L	L	H	ON	OFF	OFF	ON
L	H	H	OFF	OFF	ON	ON



Off Page Connections

From Debounce Circuit	GPIO1_43_INTn	GPIO1_43_INTn
From IO Expander	MCAN1_STB_3V3	MCAN1_STB_3V3
	MCAN0_STB_3V3	MCAN0_STB_3V3
	CAN_MUX_SEL	CAN_MUX_SEL
To HSE Connector	HSE_MCAN0_RX/UART4_TXD	HSE_MCAN0_RX/UART4_TXD
	HSE_MCAN0_TX/UART4_RXD	HSE_MCAN0_TX/UART4_RXD
	HSE_MCAN1_RX/I2C3_SDA	HSE_MCAN1_RX/I2C3_SDA
	HSE_MCAN1_TX/I2C3_SCL	HSE_MCAN1_TX/I2C3_SCL
	SOC_SPI1_CLK	SOC_SPI1_CLK
	SOC_SPI1_MOSI	SOC_SPI1_MOSI
	SOC_SPI1_MISO	SOC_SPI1_MISO
	SOC_SPI1_CS0	SOC_SPI1_CS0
	SOC_SPI1_CS1	SOC_SPI1_CS1
	SoC_I2C0_SCL	SoC_I2C0_SCL
	SoC_I2C0_SDA	SoC_I2C0_SDA
	SoC_I2C1_SCL	SoC_I2C1_SCL
	SoC_I2C1_SDA	SoC_I2C1_SDA
	CLKOUT0	CLKOUT0
To Clock Buffer	SOC_MAIN_UART0_TX_3V3	SOC_MAIN_UART0_TX_3V3
	SOC_MAIN_UART0_RX_3V3	SOC_MAIN_UART0_RX_3V3
	SOC_MAIN_UART0_CTS_3V3	SOC_MAIN_UART0_CTS_3V3
	SOC_MAIN_UART0_RTS_3V3	SOC_MAIN_UART0_RTS_3V3
To FT4232 Bridge	SOC_MAIN_UART1_TX_3V3	SOC_MAIN_UART1_TX_3V3
	SOC_MAIN_UART1_RX_3V3	SOC_MAIN_UART1_RX_3V3
	SOC_MAIN_UART3_RX_3V3	SOC_MAIN_UART3_RX_3V3
	SOC_MAIN_UART3_TX_3V3	SOC_MAIN_UART3_TX_3V3

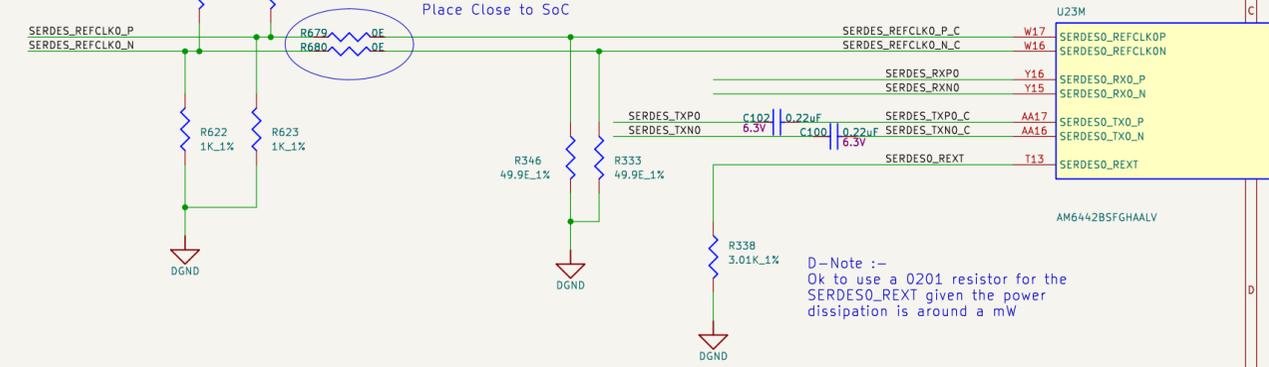
x4 Lane PCIe Connector



D-Note :-
Errata i2326 PCIe refclk Applicable?
i2326 does not apply when PCIe refclk
is from an external source. It only
applies if SK-AM64B is generating the
refclk.

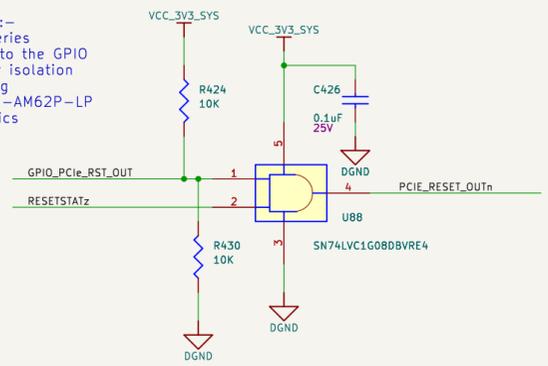
Note:
R679 , R680 Mounted with OE Resistor when PCIe REFCLK is in no Re-biasing Mode.
R679 , R680 to be replaced with 100nf CAP 0402 package when PCIe REFCLK is in
Re-biasing Mode.

CAD Note:
Place Close to SoC



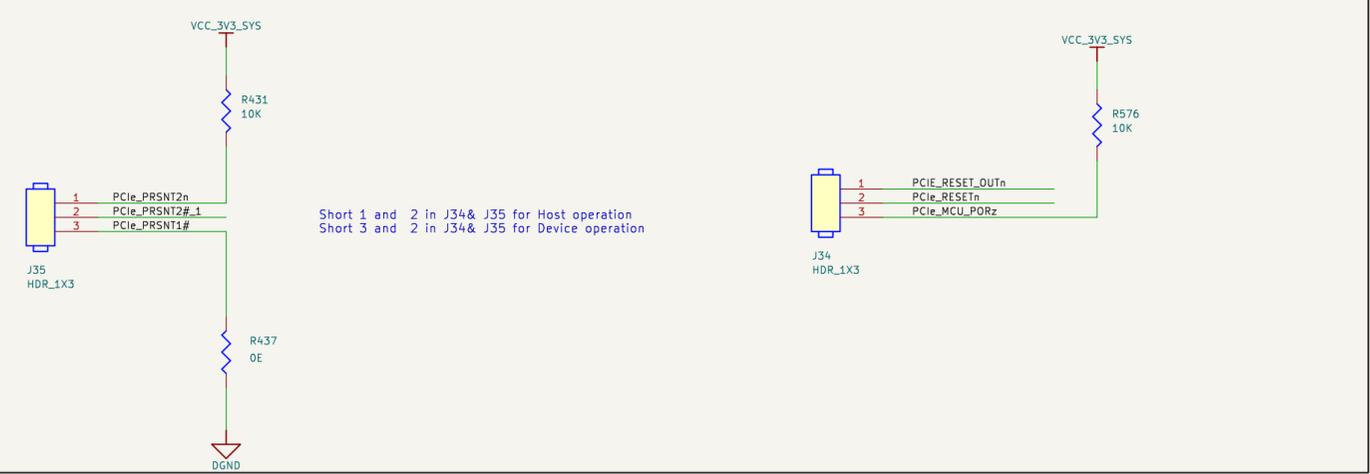
PCIe Reset

D-Note :-
Add a series
resistor to the GPIO
input for isolation
or testing
Refer SK-AM62P-LP
schematics

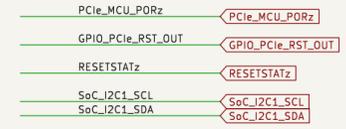


D-Note :-
SERDES0 inputs are not fail-safe.
If clock or data inputs are available before the
SOC supply ramps, VDDR_CORE rail could be
affected causing booting issues based on t

RC OR EP MODE SELECTION

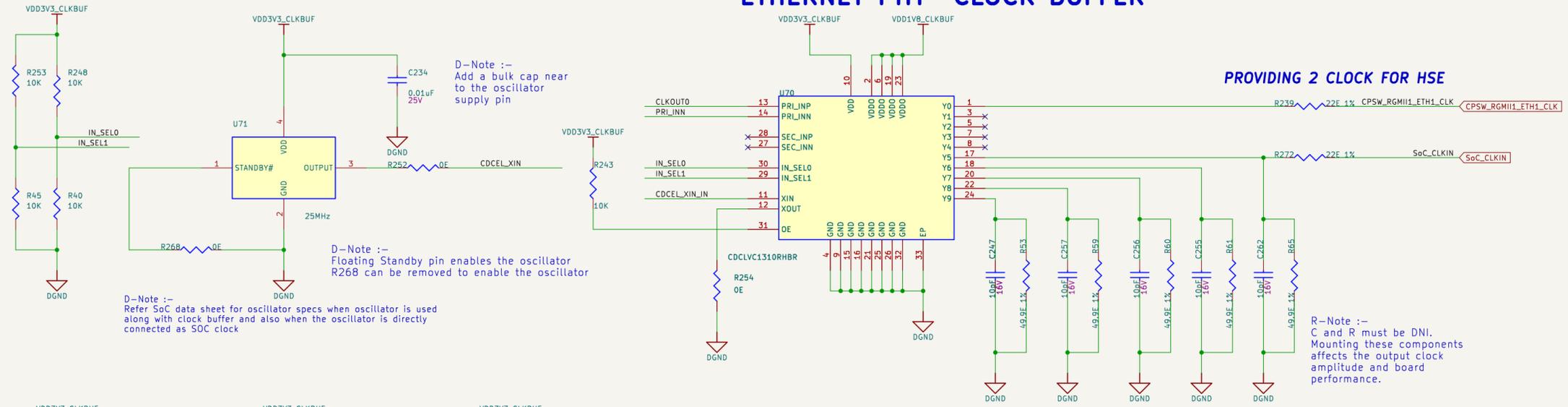


Off Page Connections

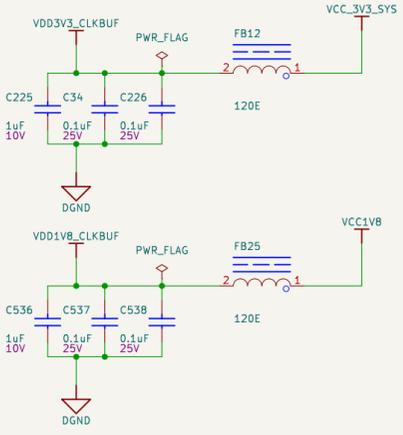


REFERENCE INPUT SELECTION

ETHERNET PHY CLOCK BUFFER



PROVIDING 2 CLOCK FOR HSE



Off Page Connections



D-Note :-
Refer SoC data sheet for oscillator specs when oscillator is used along with clock buffer and also when the oscillator is directly connected as SOC clock

D-Note :-
Floating Standby pin enables the oscillator
R268 can be removed to enable the oscillator

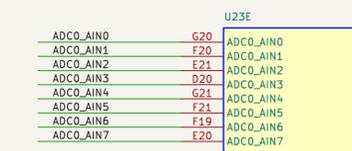
D-Note :-
Add a bulk cap near to the oscillator supply pin

R-Note :-
C and R must be DNI.
Mounting these components affects the output clock amplitude and board performance.

D-Note :-
If overdriving the oscillator stage, it is necessary to ac-couple the input with a capacitor. Otherwise, if selecting the bypass, there is no requirement for a coupling capacitor.

D-Note :-
 ADC inputs are not fail-safe. No input voltage should be apply before the SOC supply ramps. The SOC functionality could be affected if ADC inputs are applied before the SOC supply ramps
 Use a FET or similar switch to control the input voltage in case they are available before the SOC supply ramps
 The Switch needs to be enabled after the SOC supply ramps

ADC CONNECTOR



AM6442B5FGHAALV

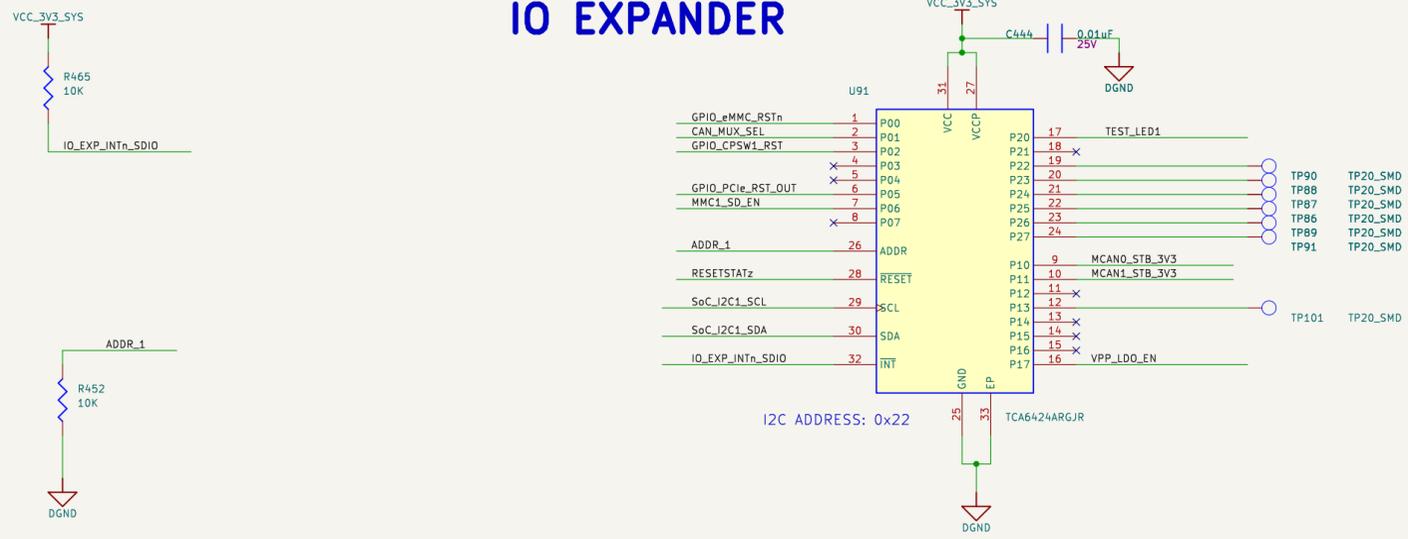
D-Note :-
 For connecting the ADC0 signals, Refer Pin connectivity table when entire ADC0 is not used or any ADC input is not used

D-Note :-
 ADC0_AIN when not used for ADC function can be used as General Purpose Input
 The assignment of each ADC0 pin to the GPIO1 module is defined in the ADC0 Signal Description table found in the data sheet.

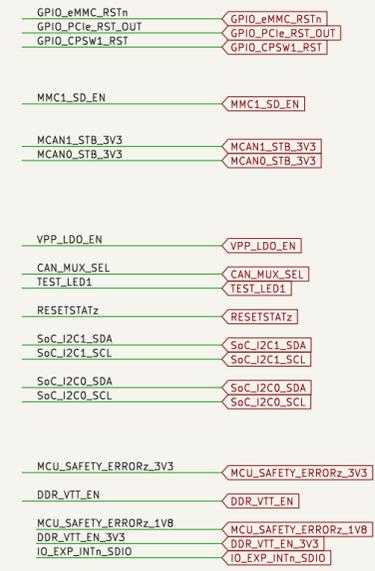
Off Page Connections



IO EXPANDER

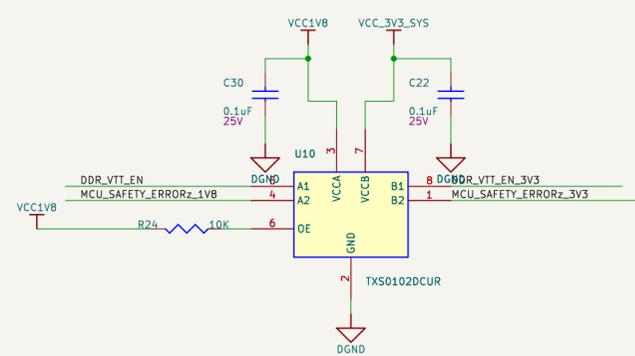


Off Page Connections

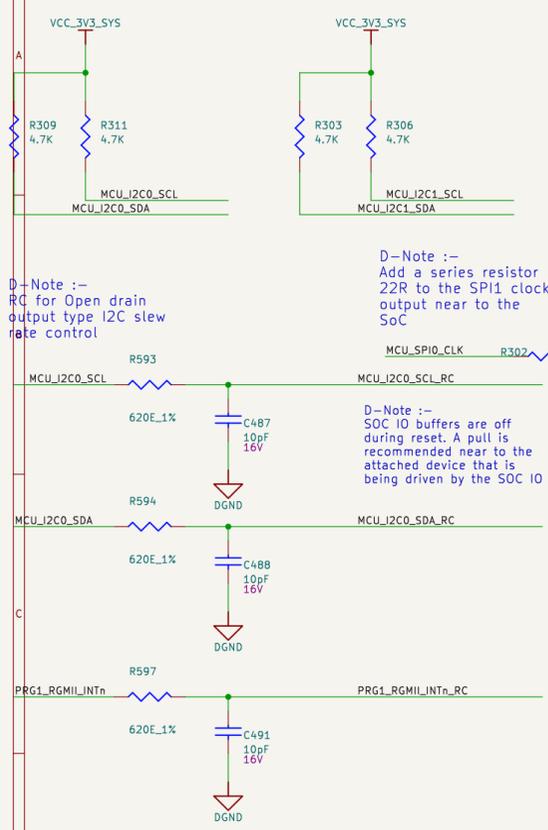


From Safety Connector
 From SoC OSPI Section
 To Processor
 To VTT Reg
 To SoC MMC

LEVEL TRANSLATOR



SOC-MCU_GENERAL



D-Note :-
RC for Open drain output type I2C slave rate control

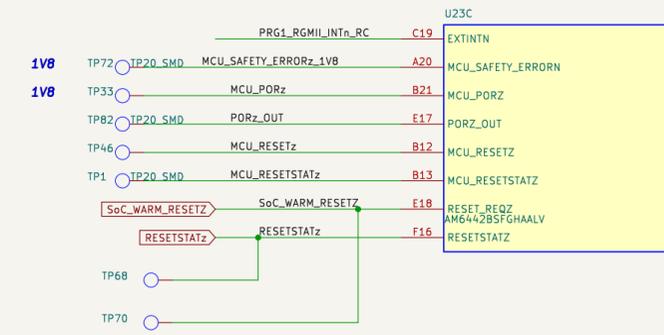
D-Note :-
Add a series resistor 22R to the SPI1 clock output near to the SoC

D-Note :-
SoC IO buffers are off during reset. A pull is recommended near to the attached device that is being driven by the SOC IO

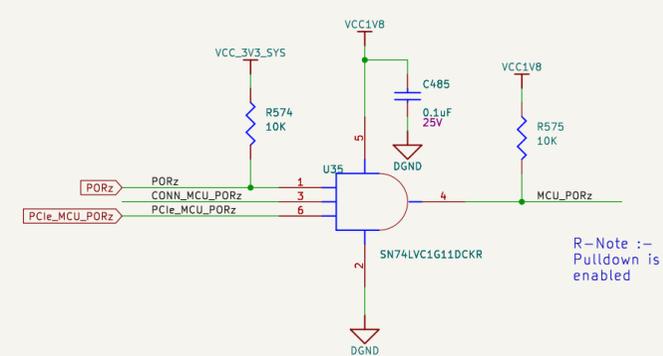
U23H		U23C	
MCU_I2C0_SCL_RC	E9	MCU_I2C0_SCL	A10
MCU_I2C0_SDA_RC	A10	MCU_I2C0_SDA	A11
MCU_I2C1_SCL	A11	MCU_I2C1_SCL	B10
MCU_I2C1_SDA	B10	MCU_I2C1_SDA	B20
MCU_OSC0_XI	C21	MCU_OSC0_XI	C21
MCU_OSC0_XO	B20	MCU_OSC0_XO	B20
MCU_SPIO_CLK	E6	MCU_SPIO_CLK	E6
MCU_SPIO_D0	E7	MCU_SPIO_D0	E7
MCU_SPIO_D1	B6	MCU_SPIO_D1	B6
MCU_SPIO_C50	D6	MCU_SPIO_C50	D6
MCU_SPIO_C51	C6	MCU_SPIO_C51	C6
MCU_GPI00_7	D7	MCU_SPH1_CLK	D7
MCU_GPI00_8	C7	MCU_SPH1_D0	C7
MCU_GPI00_9	C8	MCU_SPH1_D1	C8
TEST_LED2	A7	MCU_SPH1_C50	A7
MCU_GPI00_6	B7	MCU_SPH1_C51	B7
MCU_UART0_RX_3V3	A9	MCU_UART0_RXD	A9
MCU_UART0_TX_3V3	A8	MCU_UART0_TXD	A8
MCU_UART1_RX_3V3	C9	MCU_UART1_RXD	C9
MCU_UART1_TX_3V3	D9	MCU_UART1_TXD	D9
MCU_UART0_CTS_3V3	D8	MCU_UART0_CTSN	D8
MCU_UART0_RTS_3V3	E8	MCU_UART0_RTSN	E8
MCU_UART1_CTS_3V3	B8	MCU_UART1_CTSN	B8
MCU_UART1_RTS_3V3	B9	MCU_UART1_RTSN	B9

D-Note :-
MCU_SAFETY_ERRORz_1V8
Provision for a pulldown
Populate when attached
device is connected
Refer SOC data sheet pin
connectivity requirements

SOC RESET



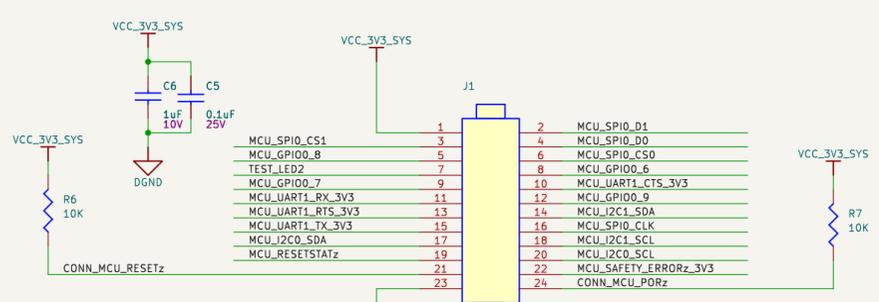
D-Note :-
It is recommended to connect the output from logic gate or discrete buffer (with fast rise time) as MCU_PORz input rather than slow rising open drain output (could glitch internally).



R-Note :-
Pull-down is enabled

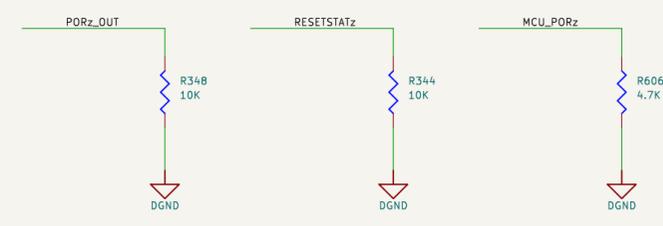
D-Note :-
Not connecting a valid MCU_PORz could cause unpredictable and probably random behavior, since the device is not getting a valid reset, internal circuits would be in random states. Slow rising reset signal could cause glitches internal to the SOC reset circuit. Use a discrete buffer and have the fast rising output of the buffer drive the MCU_PORz is recommended

SOC - MCU (SAFETY) CONNECTOR



D-Note :-
Processor IOs connected to MCU expansion CONNECTOR are not fail-safe. No external input shall be applied when Starter Kit/EVM is not powered-up

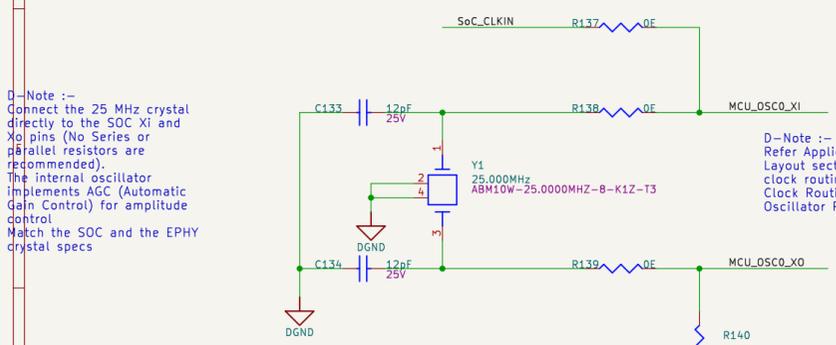
D-Note :-
MCU_PORz pull-down is used to hold the SOC in reset during power-up



D-Note :-
Pull-down resistors on PORz_OUT and RESEtSTATz are provided to keep the signal low until the processor is released from reset during the power-up sequence

CRYSTAL FOR SOC MCU_OSC0

LPF Designed for 25MHz Cutoff
Have to change resistor and capacitor values accordingly

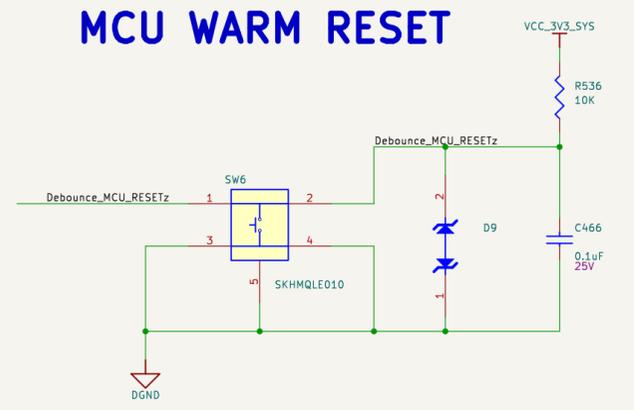


D-Note :-
Connect the 25 MHz crystal directly to the SOC XI and XO pins (No Series or parallel resistors are recommended). The internal oscillator implements AGC (Automatic Gain Control) for amplitude control. Match the SOC and the EPHY crystal specs

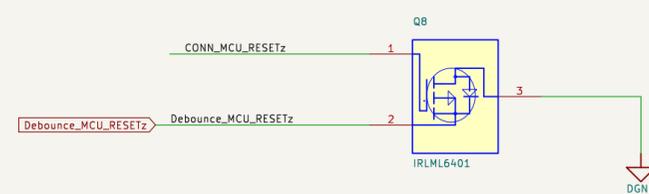
D-Note :-
Refer Applications, Implementation, and Layout section of the data sheet for clock routing guidelines as below:
Clock Routing Guidelines
Oscillator Routing

D-Note :-
XO should be grounded when an external oscillator is used
Refer SOC data sheet

MCU WARM RESET



D-Note :-
No HFOSC0 registers are required to be changed. These registers should remain in their default state. Select the appropriate crystal circuit components that are compliant to the values defined in the MCU_OSC0 Crystal Circuit Requirements table. Read the Load Capacitance and Shunt Capacitance sections to select the appropriate crystal circuit components.

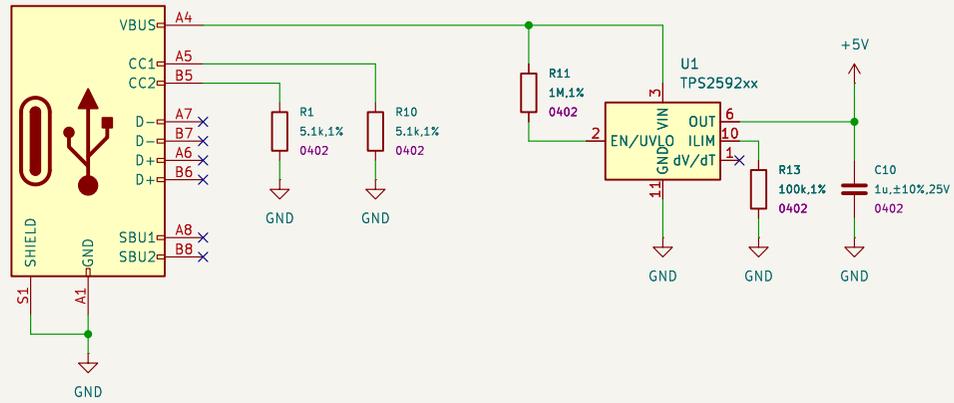


Off Page Connections

MCU_PORz	MCU_PORz
MCU_RESEtZ	MCU_RESEtZ
MCU_RESEtSTATz	MCU_RESEtSTATz
MCU_SAFETY_ERRORz_3V3	MCU_SAFETY_ERRORz_3V3
MCU_SAFETY_ERRORz_1V8	MCU_SAFETY_ERRORz_1V8
PORz_OUT	PORz_OUT
RESEtSTATz	RESEtSTATz
PRG1_RGMII_INTn	PRG1_RGMII_INTn
TEST_LED2	TEST_LED2
MCU_GPI00_6	MCU_GPI00_6
SoC_CLKIN	SoC_CLKIN
MCU_UART0_TX_3V3	MCU_UART0_TX_3V3
MCU_UART0_RX_3V3	MCU_UART0_RX_3V3
MCU_UART0_CTS_3V3	MCU_UART0_CTS_3V3
MCU_UART0_RTS_3V3	MCU_UART0_RTS_3V3

To HSE Connector
To level translator
From Level Translator
To Boot Mode Section
From ICSSG Phy1&2
To User LED
From Push button Switch

J2
 USB_C_U262-161N-4BVC11
 USB_C_20
 KKB
 U262-161N-4BVC11
 C319148



Sheet: /usb-power-efuse/
 File: usb-power-efuse.kicad_sch

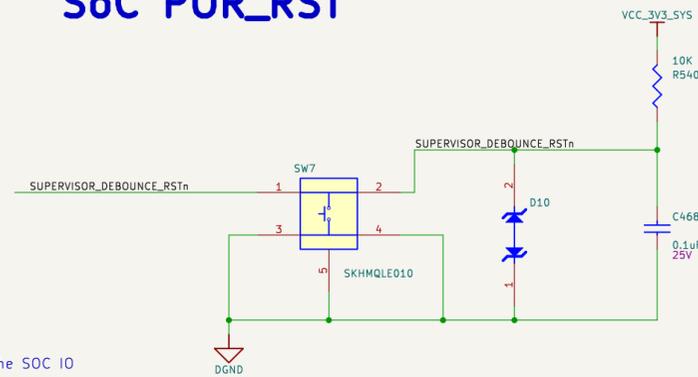
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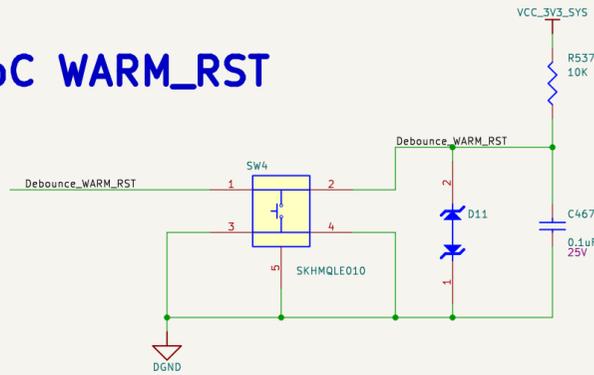
Rev:
 Id: 29/28

SoC POR_RST

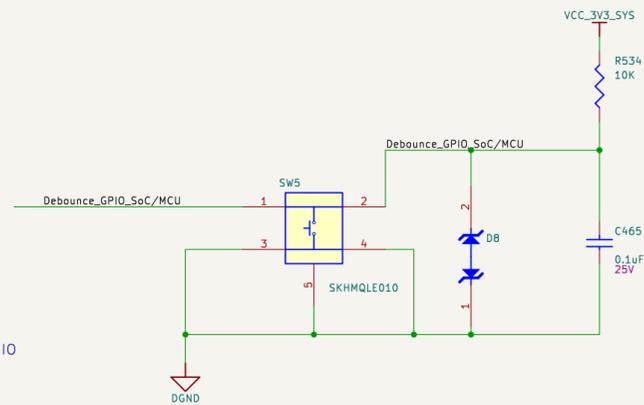


Cad Note :-
Place ESD diode near to the SOC IO

SoC WARM_RST



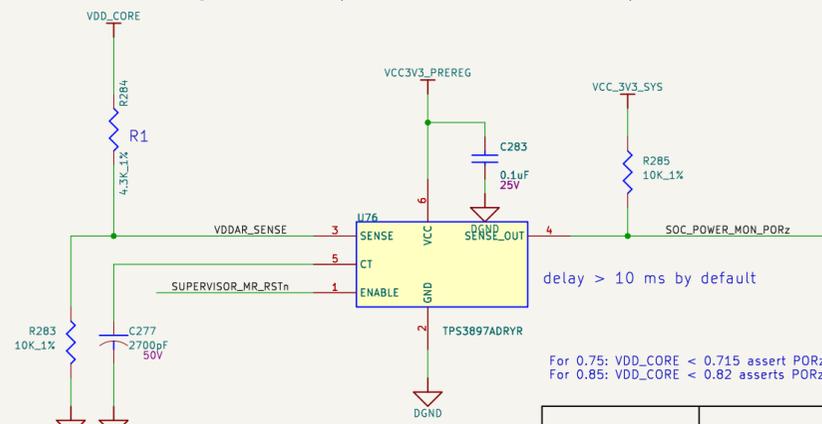
Cad Note :-
Place ESD diode near to the SOC IO



Cad Note :-
Place ESD diode near to the SOC IO

VOLTAGE SUPERVISOR

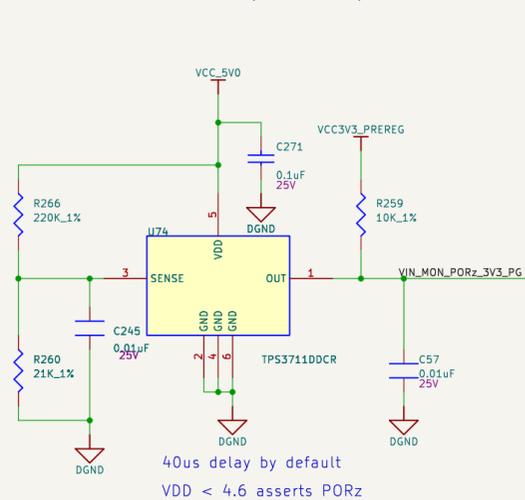
Core Voltage Monitor (VDDAR_CORE/VDD_CORE)



delay > 10 ms by default
For 0.75: VDD_CORE < 0.715 asserts PORz
For 0.85: VDD_CORE < 0.82 asserts PORz

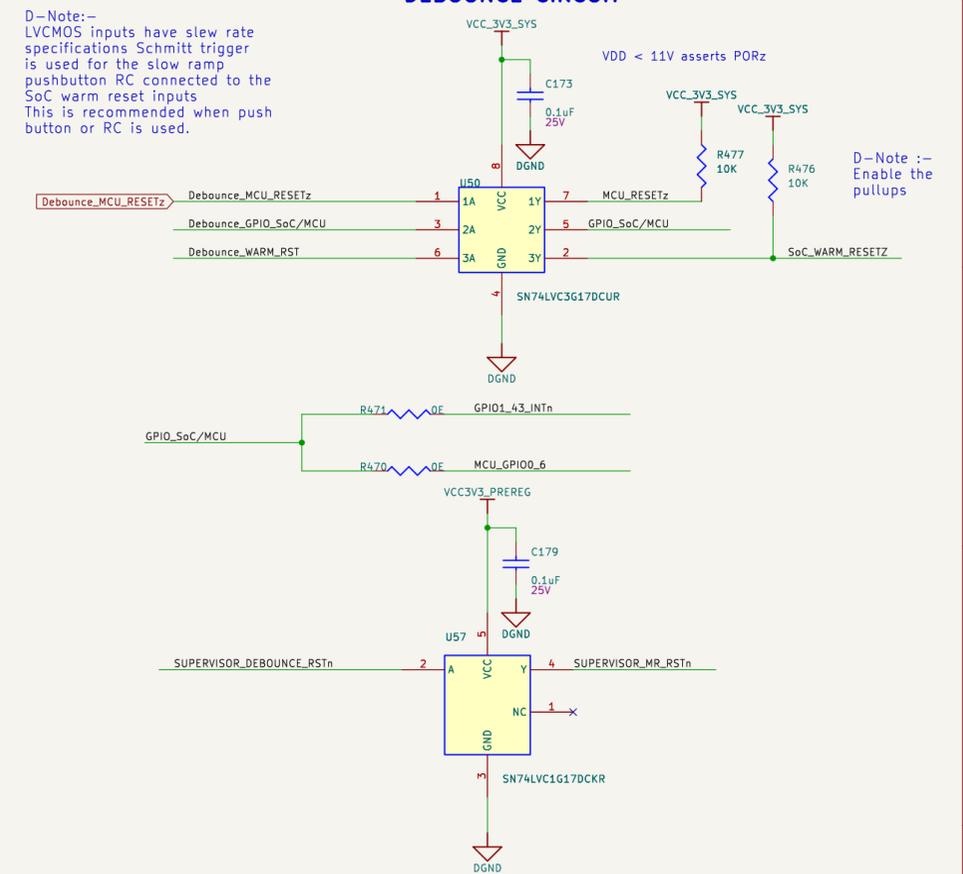
CORE VOLTAGE	RES TO BE PLACED
0.75V	R1 = 4.3K
0.85V	R2 = 6.34K

5V OUTPUT MONITOR (VCC_5V0)



40us delay by default
VDD < 4.6 asserts PORz

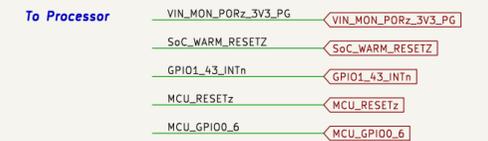
DEBOUNCE CIRCUIT



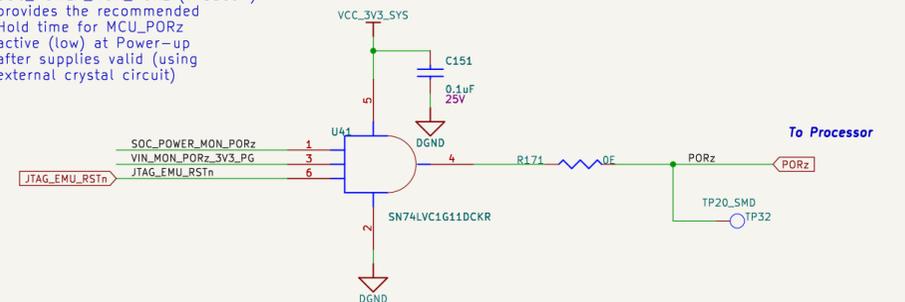
D-Note :-
LVCMOS inputs have slew rate specifications Schmitt trigger is used for the slow ramp pushbutton RC connected to the SoC warm reset inputs This is recommended when push button or RC is used.

D-Note :-
Enable the pullups

Off Page Connections

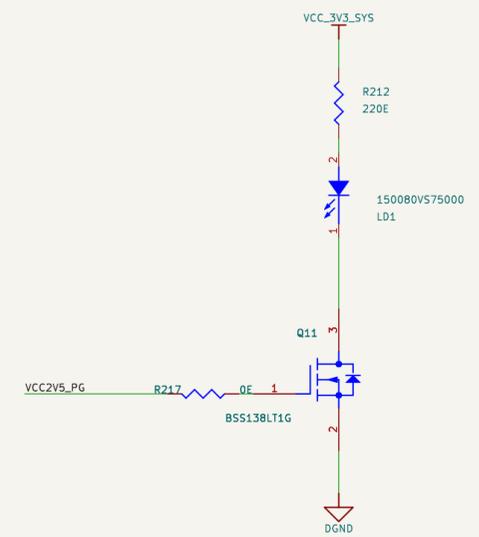


D-Note :-
SOC_POWER_MON_PORz (TPS3897) provides the recommended Hold time for MCU_PORz active (low) at Power-up after supplies valid (using external crystal circuit)

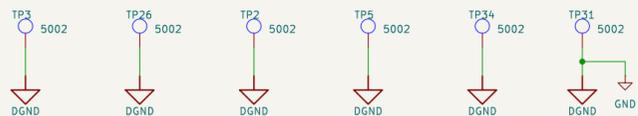


MAIN INPUT 12V DC

POWER INDICATION LED's



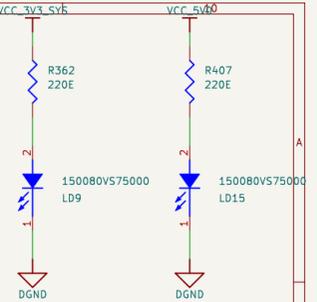
Ground test points



Off Page Connections

VCC_CORE_PG — VCC_CORE_PG

VCC2V5_PG — VCC2V5_PG



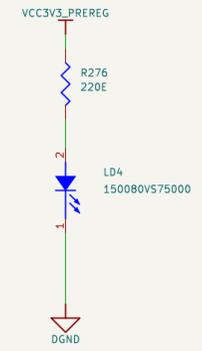
D-Note :-
Iout for 5V is Considered as 3A Max

Off Page Connections



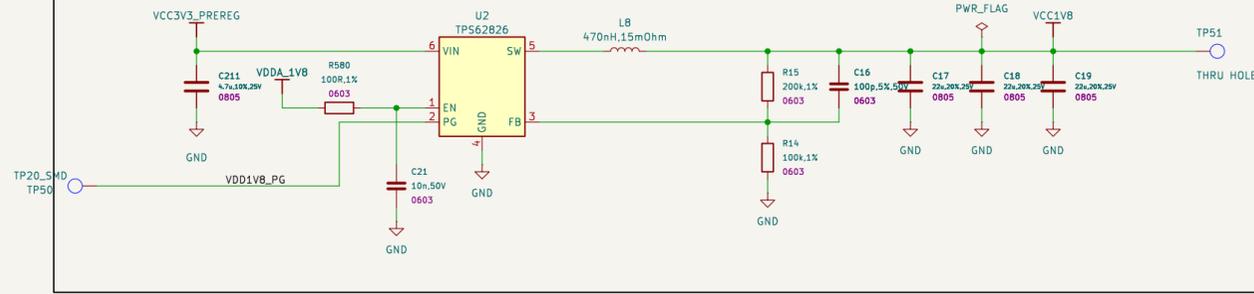
PREREG 3.3V, 3.0AMPS SUPPLY

D-Note :-
Add a Jumper or OR
for isolation or
Current measurement
for preproduction
board

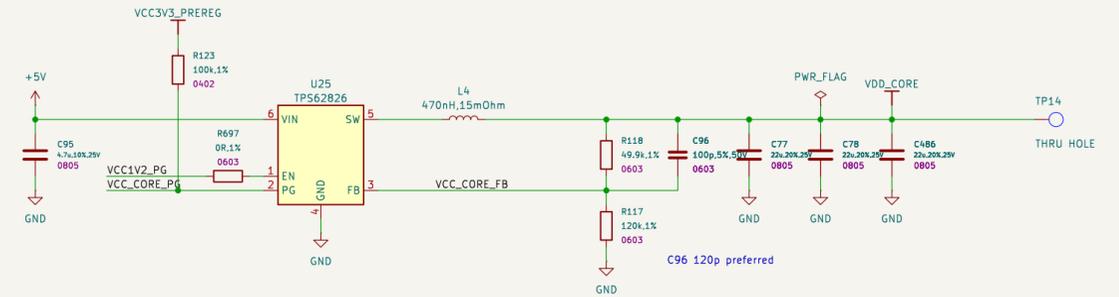


SoC POWER SUPPLIES

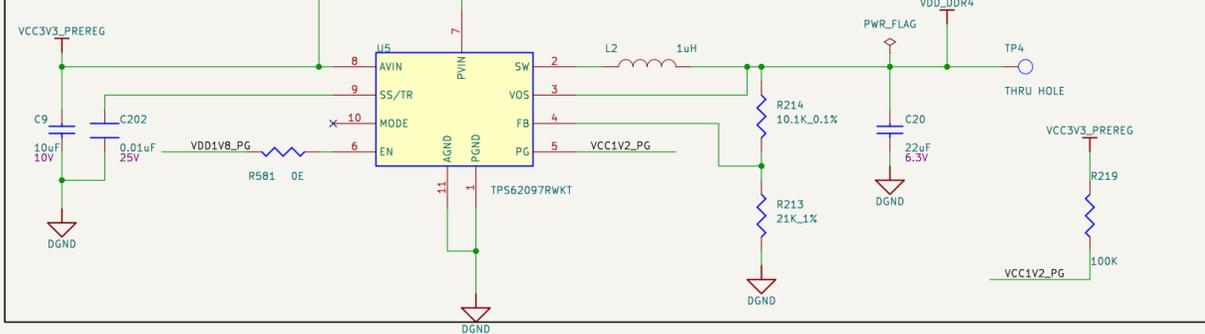
1.8V IO, 3.0 AMPS SUPPLY



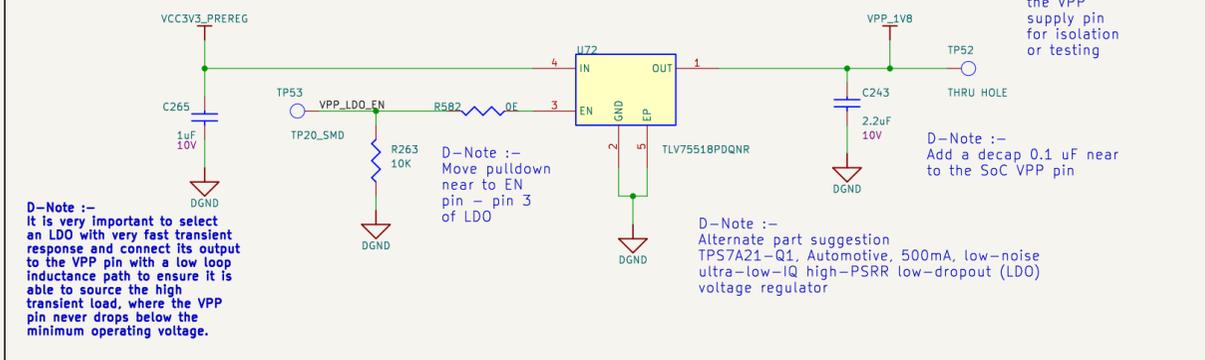
0.75 /0.85V, 3.0 AMPS SUPPLY



1.2V, 2.0 AMPS SUPPLY



1.8V VPP, 0.5 AMP SUPPLY



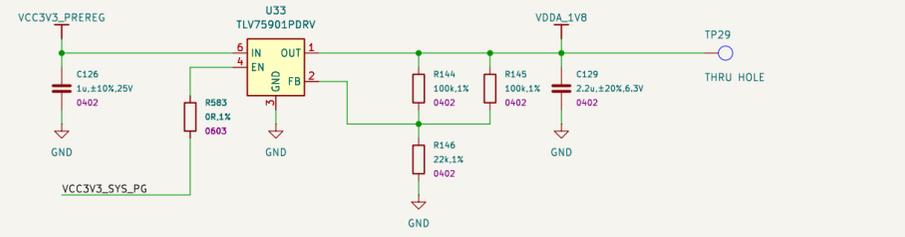
D-Note :-
An alternative way to source the VPP is to use an external supply. The required caps and termination/Discharge resistor are recommended to be placed near to the SoC VPP pin. SoC GPIO output can be used to control or time the external power supply output

D-Note :-
Given the transient current requirement during eFuse programming, using load switch or FET switch may not be a recommended approach. It is recommended to use an LDO. A load or FET switch is likely to have too much voltage drop that can't be compensated like when using an LDO.

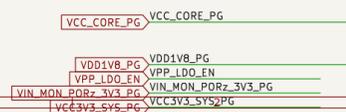
1.8V Analog , 1 AMP SUPPLY

This chip has no PowerGood output, which is logically ANDed with VCC1V8_PG (from DCDC) for DDR power enable in original design.

We change the concurrent VCC1V8 and VDDA_1V8 ramps to sequential one, first VDDA_1V8 then VCC1V8.

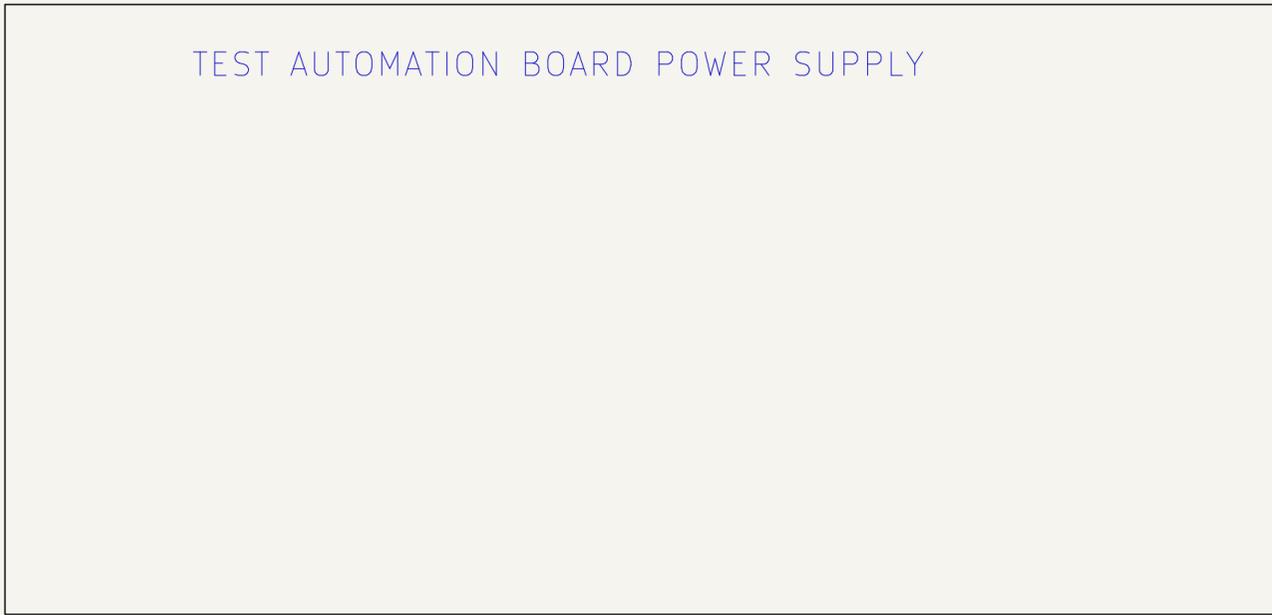


Off Page Connections

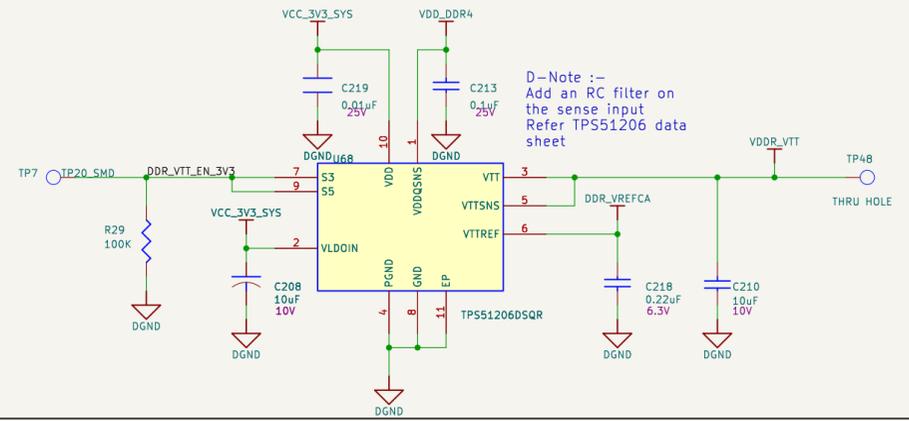


PERIPHERAL POWER SUPPLIES

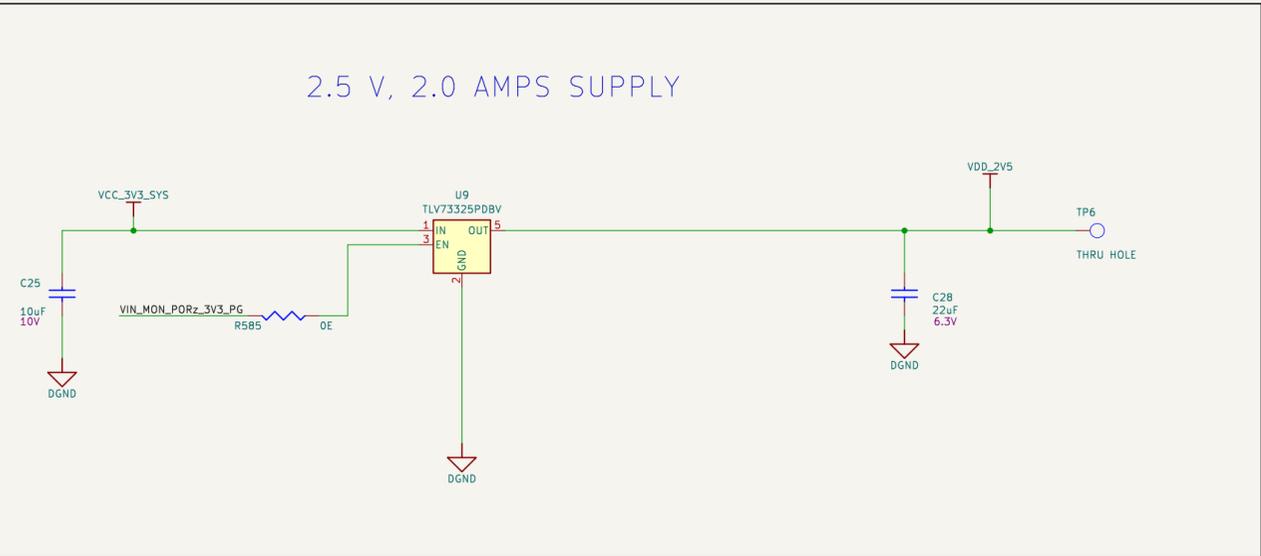
TEST AUTOMATION BOARD POWER SUPPLY



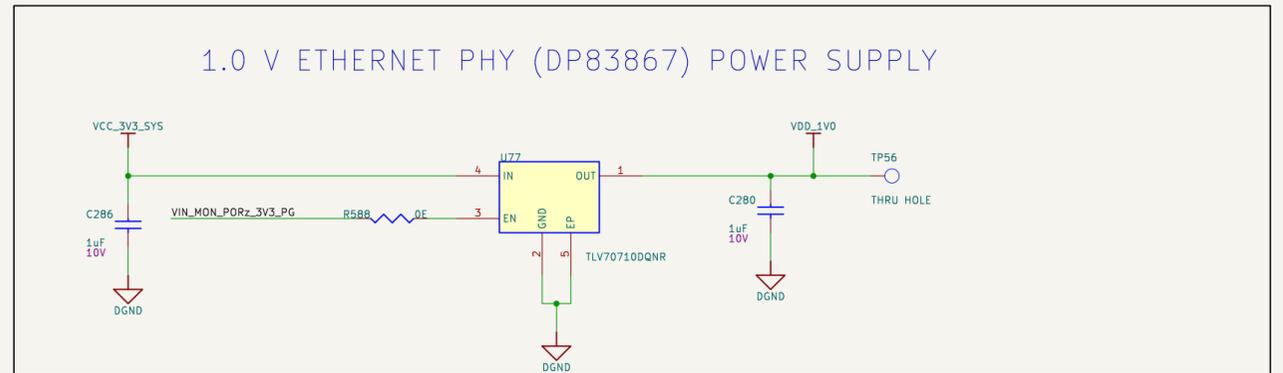
VTT SUPPLY FOR DDR4



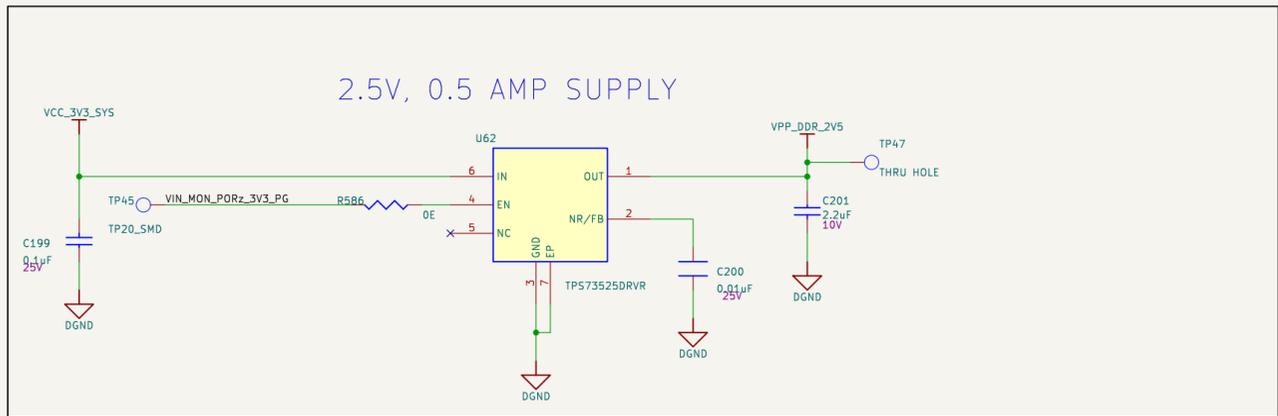
2.5 V, 2.0 AMPS SUPPLY



1.0 V ETHERNET PHY (DP83867) POWER SUPPLY



2.5V, 0.5 AMP SUPPLY



Off Page Connections

DDR_VTT_EN_3V3	DDR_VTT_EN_3V3
VCC2V5_PG	VCC2V5_PG
VCC3V3_SYS_PG	VCC3V3_SYS_PG
VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG

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Id: 33/28

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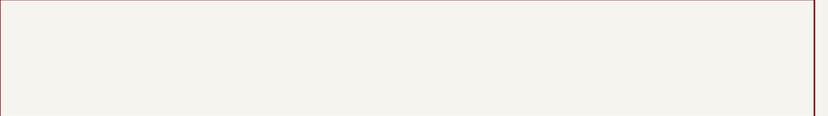
-  H1
MountingHole
-  H2
MountingHole
-  H3
MountingHole
-  H4
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-  H5
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-  H6
MountingHole
-  H7
MountingHole
-  H8
MountingHole
-  H9
MountingHole
-  H10
MountingHole
-  H11
MountingHole
-  H12
MountingHole
-  H13
MountingHole

B

C

D

1 2 3 4 5 6



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