

Power

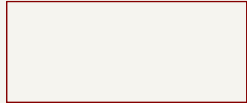
Voltage Regulators - 3V3, 1V8, 1V0



File: pd.kicad_sch

Decaps

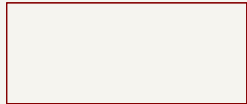
Decaps



File: decap.kicad_sch

Config + Programming

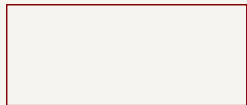
Config + Programming



File: peripherals.kicad_sch

Board -> Outside World

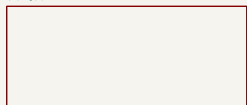
Pinout



File: pinout_external.kicad_sch

FPGA

FPGA



File: fpga.kicad_sch

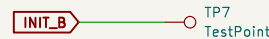
Status LEDs/test points

DONE



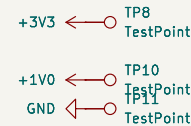
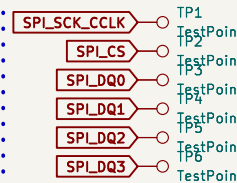
The DONE pin has an internal 10k pull-up resistor. It is pulled high when config is finished.

INIT

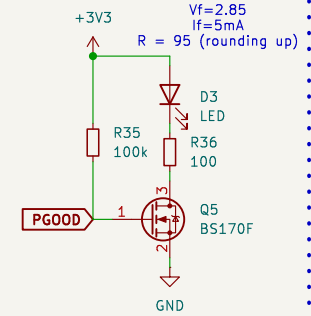


When pulled high the FPGA proceeds with configured initialization per M[2:0] pins. Expose a test pad here

SPI testpoints



Power Indicator



To look at subsheets,
double click the above boxes
or use the left "Schematic Hierarchy"
pane to click on them.

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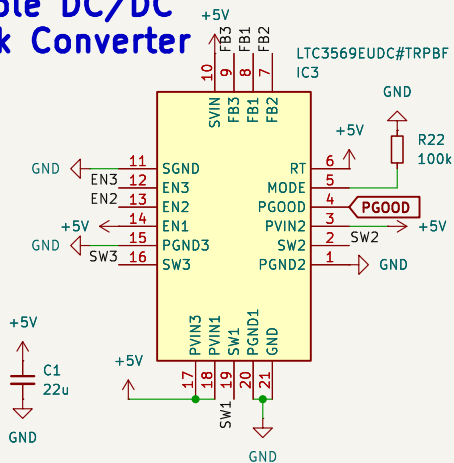
Sheet: /
File: sip-board.kicad_sch

Title: Z80 Drop In SiP Board

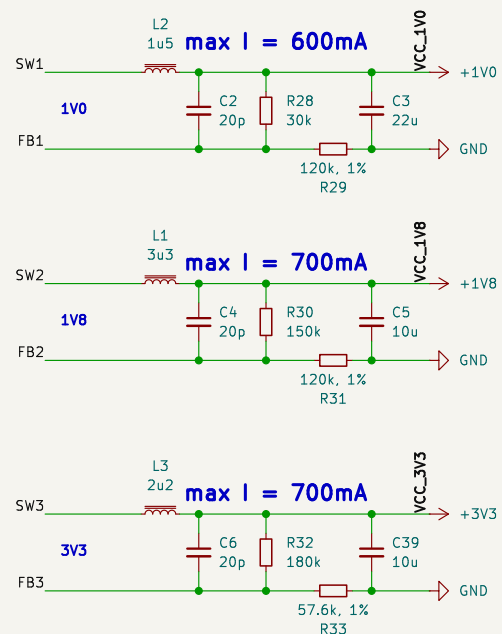
Size: A4 Date:
KiCad E.D.A. 9.0.0

Rev: 3
Id: 1/6

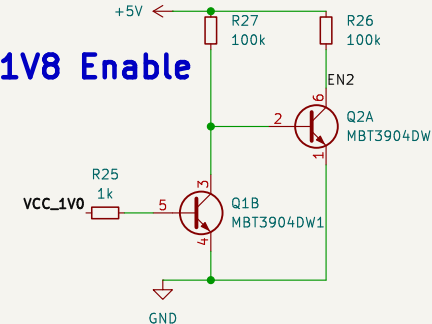
Triple DC/DC Buck Converter



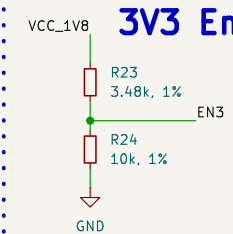
Output/Feedback



1V8 Enable



3V3 Enable



https://s3-us-west-2.amazonaws.com/digilent/resources/programmable-logic/cmod-s7/Cmod+S7_sch-public.pdf

The recommended power-on sequence is VCCINT, VCCBRAM, VCCAUX, and VCCO to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If VCCINT and VCCBRAM have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If VCCAUX and VCCO have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For VCCO voltages of 3.3V in HR I/O banks and configuration bank 0 the following conditions apply.

- The voltage difference between VCCO and VCCAUX must not exceed 2.625V for longer than TVCC02VCCAUX for each power-on/off cycle to maintain device reliability levels.
- The TVCC02VCCAUX time can be allocated in any percentage between the power-on and power-off ramps.

There is no recommended sequence for supplies not discussed in this section.

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Sheet: /Voltage Regulators - 3V3, 1V8, 1V0/
File: pd.kicad_sch

Title:

Size: A4
KiCad E.D.A. 9.0.0

Date:

Rev:
Id: 2/6

Decoupling Capacitors

XC7 PCB guide

https://docs.amd.com/v/u/en-US/ug483_7Series_PCB

XC7 Config

https://docs.amd.com/v/u/en-US/ug470_7Series_Config

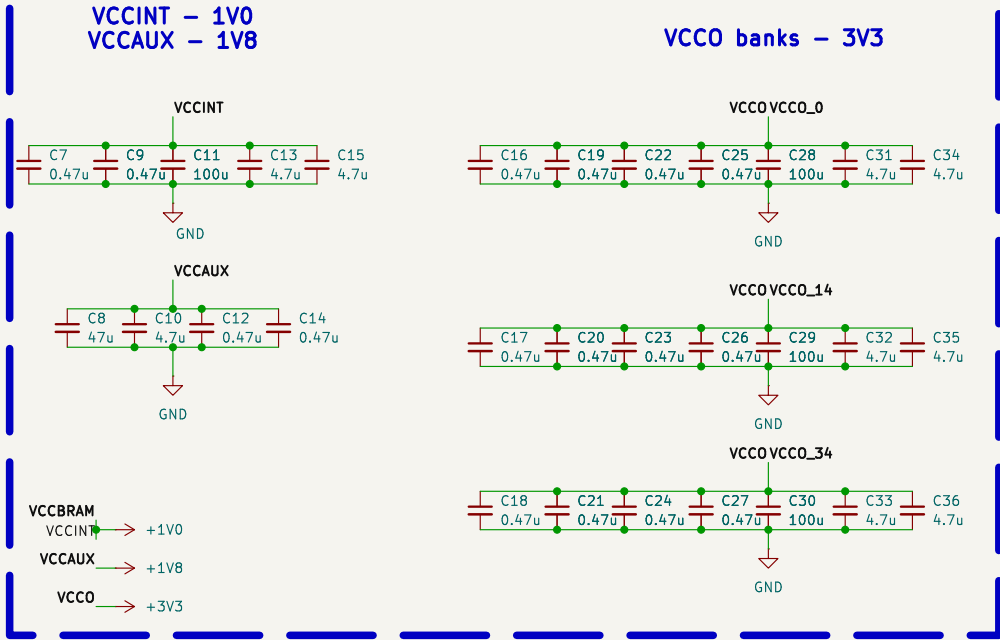


Table 2-1: Required PCB Capacitor Quantities per Device: Spartan-7 Devices⁽¹⁾⁽²⁾

Package	Device	V _{CCINT}				V _{CCBRAM}				V _{CCAUX}			V _{CCO} (per Bank)		
		330 μF	100 μF	4.7 μF	0.47 μF	100 μF	47 μF	4.7 μF	0.47 μF	47 μF	4.7 μF	0.47 μF	47 μF or 100 μF ⁽³⁾	4.7 μF	0.47 μF
CPGA196	XC7S6	0	1	1	1	0	1	1	1	1	1	2	1	2	4
CSGA225	XC7S6	0	1	1	1	0	1	1	1	1	1	2	1	2	4
FTGB196	XC7S6	0	1	1	1	0	1	1	1	1	1	2	1	2	4
CPGA196	XC7S15	0	1	2	2	0	1	1	1	1	1	2	1	2	4

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Sheet: /Decaps/
File: decap.kicad_sch

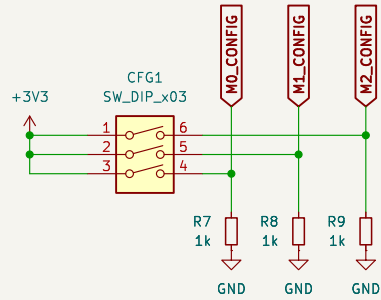
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KiCad E.D.A. 9.0.0

Date:

Rev:
Id: 3/6

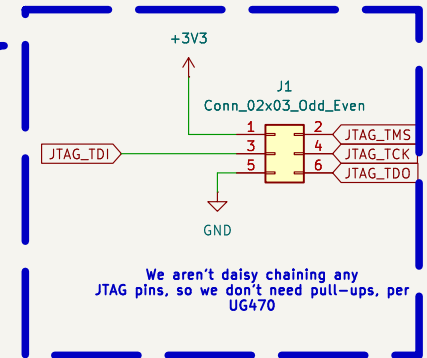
Boot Configuration



M[2:0] = 001 for Master SPI config

M[2:0] = 101 for JTAG programming

JTAG Connector

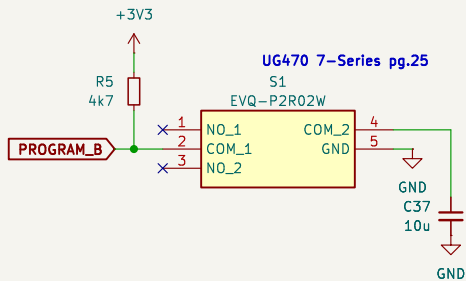


We aren't daisy chaining any JTAG pins, so we don't need pull-ups, per UG470

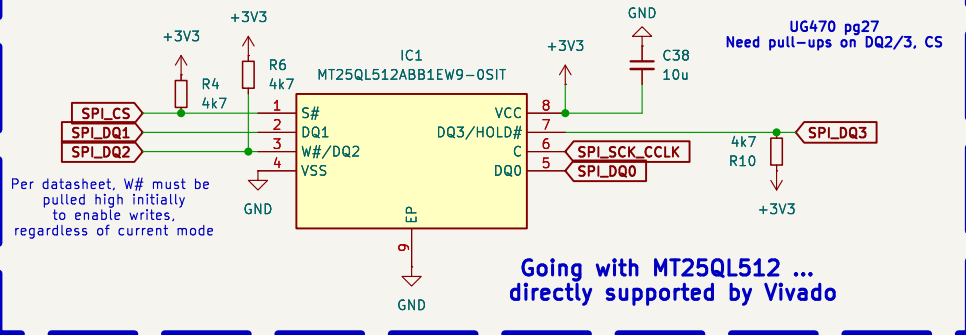
<https://www.tag-connect.com/wp-content/uploads/bsk-pdf-manager/2019/12/>

Reset Logic

Active low



SPI Memory



Per datasheet, W# must be pulled high initially to enable writes, regardless of current mode

Going with MT25QL512 ... directly supported by Vivado

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Sheet: /Config + Programming/
File: peripherals.kicad_sch

Title:

Size: A4
KiCad E.D.A. 9.0.0

Date:

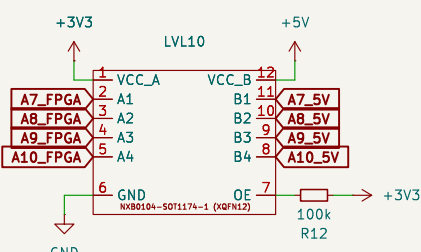
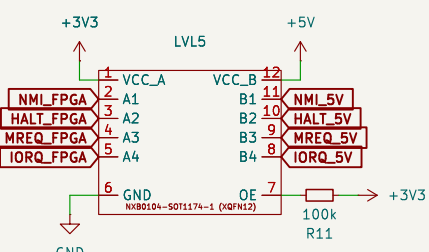
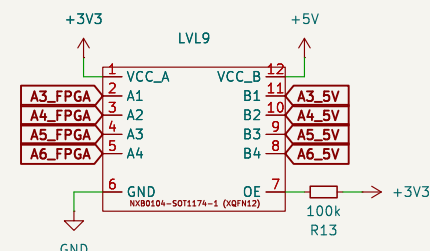
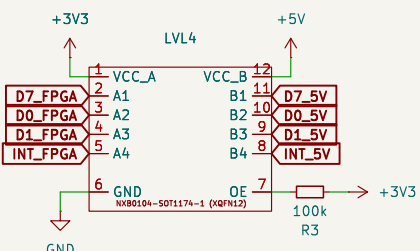
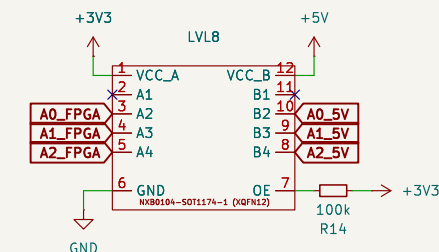
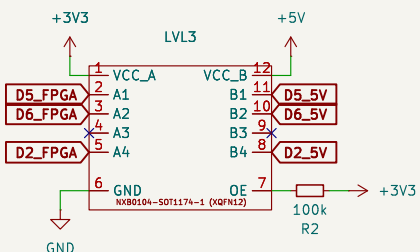
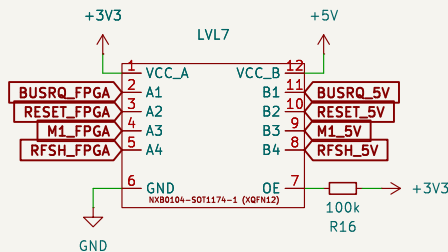
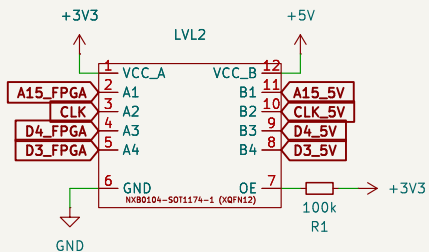
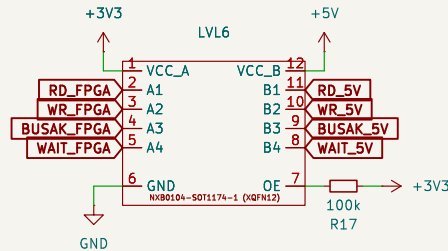
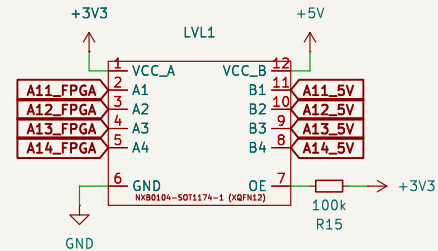
Rev:
Id: 4/6

Pins 1-20 We want pullup on OE
(ascending order)

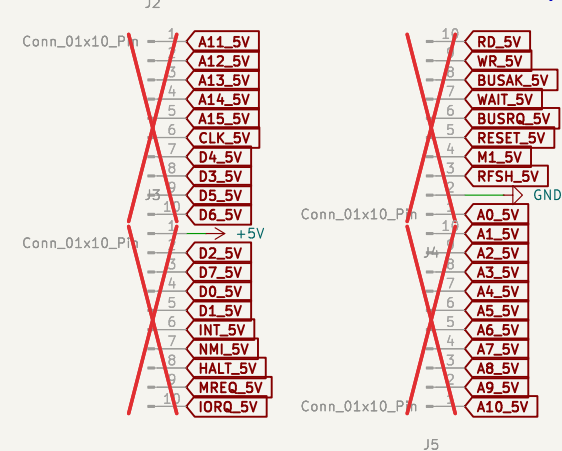
Pins 21-40
(ascending order)

**3V3 <-> 5V level shifters
(FPGA <-> Z80 System)**

Right side of board's pinouts might need to be vertically swapped due to rotation/flipping of level shifters - TBD



**Z80 System Connectors
DNP - castellated hole footprint**



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Sheet: /Pinout/ File: pinout_external.kicad_sch		
Title:		
Size: A4	Date:	Rev:
KiCad E.D.A. 9.0.0		Id: 5/6

FPGA – XC7S15CPGA196

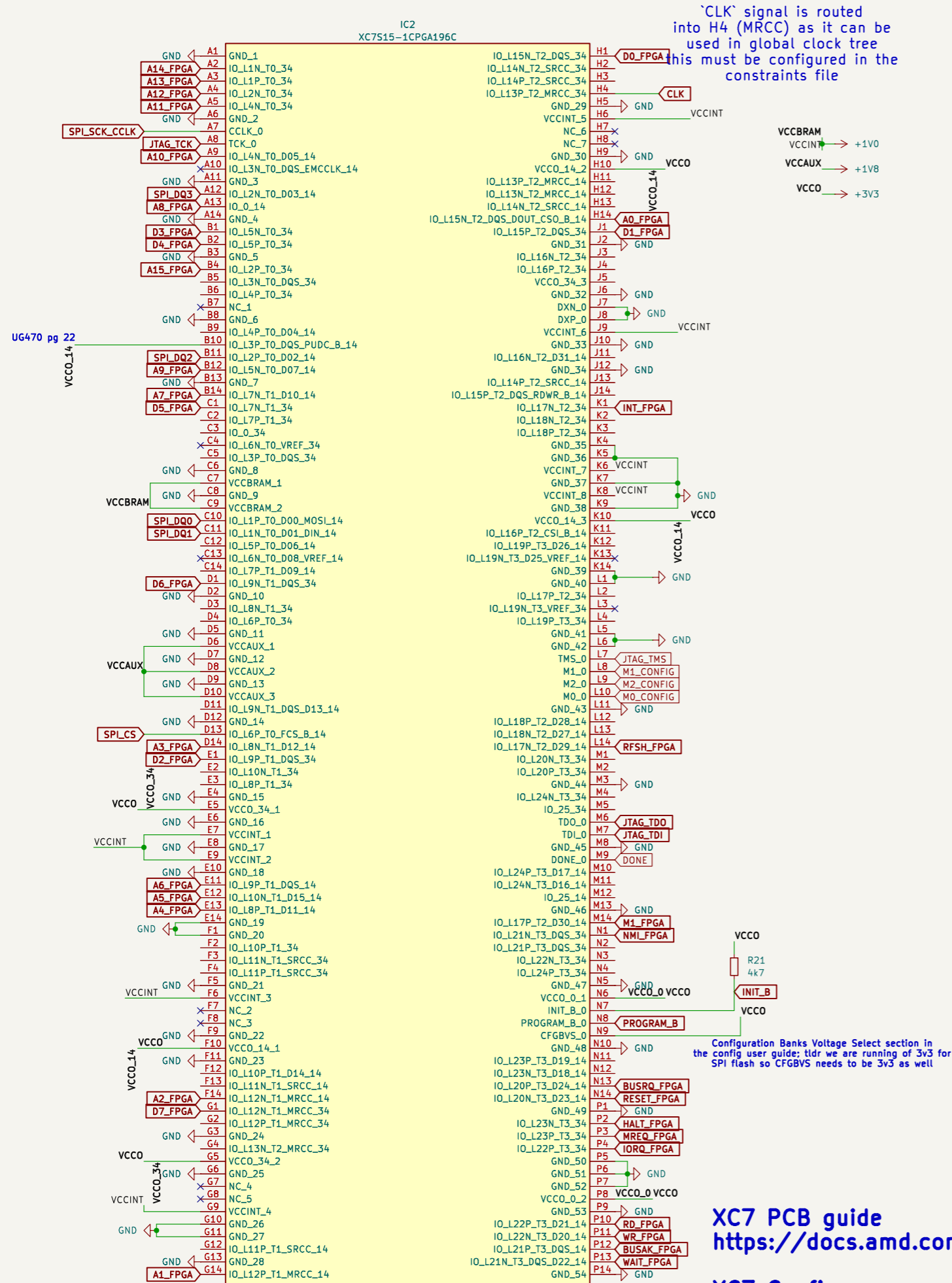


Table 2-2: Configuration Mode Pins (Table 1 of 2)

Pin Name	Bank	JTAG (Only)	Slave Serial	Master Serial	Master SPI		
					x1	x2	x4
CFGBVS	0	CFGBVS	CFGBVS	CFGBVS	CFGBVS	CFGBVS	CFGBVS
M[2:0]	0	M[2:0]=101	M[2:0]=111	M[2:0]=000	M[2:0]=001	M[2:0]=001	M[2:0]=001
TCK	0	TCK	TCK	TCK	TCK	TCK	TCK
TMS	0	TMS	TMS	TMS	TMS	TMS	TMS
TDI	0	TDI	TDI	TDI	TDI	TDI	TDI
TDO	0	TDO	TDO	TDO	TDO	TDO	TDO
PROGRAM_B	0	PROGRAM_B	PROGRAM_B	PROGRAM_B	PROGRAM_B	PROGRAM_B	PROGRAM_B
INIT_B	0	INIT_B	INIT_B	INIT_B	INIT_B	INIT_B	INIT_B
DONE	0	DONE	DONE	DONE	DONE	DONE	DONE
CCLK	0	CCLK	CCLK	CCLK	CCLK	CCLK	CCLK

FPGA Logic

Supply	Description	0.95	1.00	1.05	V
VCCINT ⁽³⁾	For -2 and -1 (1.0V) devices: internal supply voltage.	0.95	1.00	1.05	V
	For -1L (0.95V) devices: internal supply voltage.	0.92	0.95	0.98	V
VCCAUX	Auxiliary supply voltage.	1.71	1.80	1.89	V
VCCBRAM ⁽³⁾	For -2 and -1 (1.0V) devices: block RAM supply voltage.	0.95	1.00	1.05	V
	For -1L (0.95V) devices: block RAM supply voltage.	0.92	0.95	0.98	V
VCCO ⁽⁴⁾⁽⁵⁾	Supply voltage for HR I/O banks.	1.14	-	3.465	V
V _{IN} ⁽⁶⁾	I/O input voltage.	-0.20	-	V _{CCO} + 0.20	V
	I/O input voltage (when V _{CCO} = 3.3V) for V _{REF} and differential I/O standards except TMDS_33.	-0.20	-	2.625	V
I _{IN} ⁽⁸⁾	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	-	-	10	mA
VCCBATT ⁽⁹⁾	Battery voltage.	1.0	-	1.89	V

Table 2-1: Required PCB Capacitor Quantities per Device: Spartan-7 Devices⁽¹⁾⁽²⁾

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		330 µF	100 µF	4.7 µF	0.47 µF	100 µF	47 µF	4.7 µF	0.47 µF	47 µF	4.7 µF	0.47 µF	47 µF or 100 µF ⁽³⁾	4.7 µF	0.47 µF
CPGA196	XC7S6	0	1	1	1	0	1	1	1	1	1	2	1	2	4
CSGA225	XC7S6	0	1	1	1	0	1	1	1	1	1	2	1	2	4
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CPGA196	XC7S15	0	1	2	2	0	1	1	1	1	1	2	1	2	4

PAGE 21 ONWARDS
https://docs.amd.com/v/u/en-US/ug475_7Series_Pkg_Pinout

XC7 PCB guide
https://docs.amd.com/v/u/en-US/ug483_7Series_PCB
 XC7 Config
https://docs.amd.com/v/u/en-US/ug470_7Series_Config