

ULX4M-LS v004

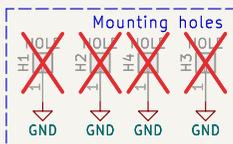
2026-02-17

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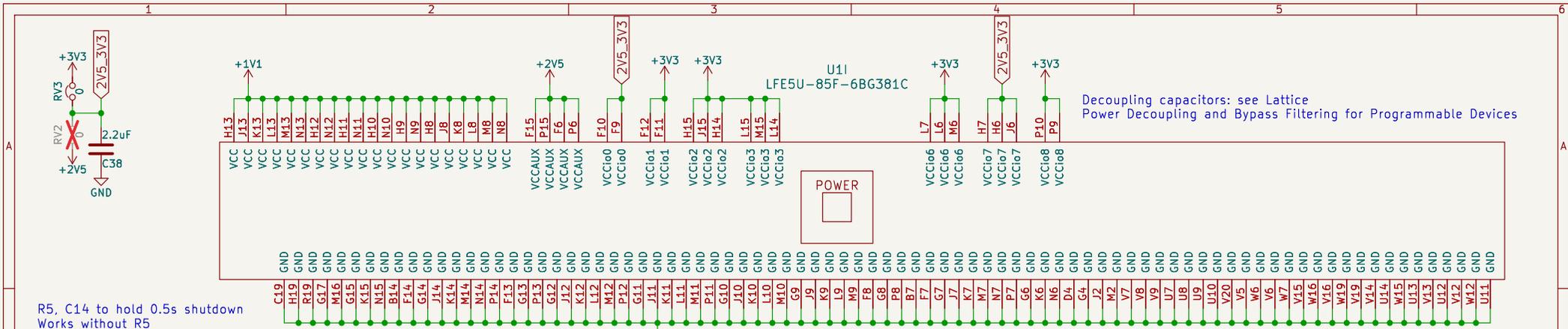
click on mouse pointer arrow on top of right toolbar
and double-click on sheet to open

power BANK POWER 3V3 2V5 1V1/1V2 1V35(DNP) File: power.kicad_sch	gpio BANK0 BANK7 CM4 connector File: gpio.kicad_sch
usb BANK6 USB DSI File: usb.kicad_sch	gpdI BANK1 SW DSI File: gpdI.kicad_sch
blinky 3X BTN 8X LED File: blinky.kicad_sch	ethernet ETHERNET (LAN8720A) File: ethernet.kicad_sch
ram BANK2 BANK3 File: ram.kicad_sch	SDRAM SDRAM (B425143209) File: ddr3.kicad_sch
serdes SERDES File: serdes.kicad_sch	flash BANK8 FLASH (IS25LP128F) File: flash.kicad_sch
MechanicalDrawings File: mek.kicad_sch	

Page	Index
.....
CoverPage	1
PowerPage	2
GPIO	3
USB	4
GPDI	5
Blinky	6
Ethernet	7
SDRAM FPGA	8
SDRAM	9
SerDes	10
Flash	11
MechanicalDrawing	12
.....



	
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Sheet: /	
File: ulx4m.kicad_sch	
Title: ULX4M-LS	
Size: A4	Date: 2025-04-05
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	Id: 1/12

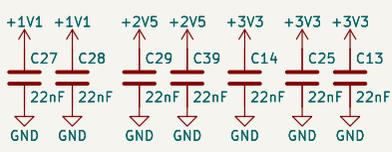
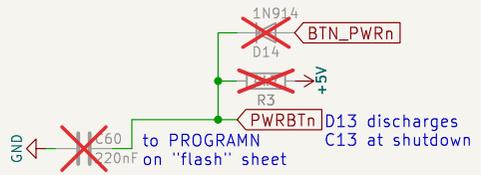


R5, C14 to hold 0.5s shutdown
Works without R5

RC network for proper switchover
to battery at fast fall of VDD.
See page 54 NXP PCF8523T datasheet.
RTC can also be powered from 2.5V
but it is easier to route 3.3V

WAKEUPn
open drain
active low

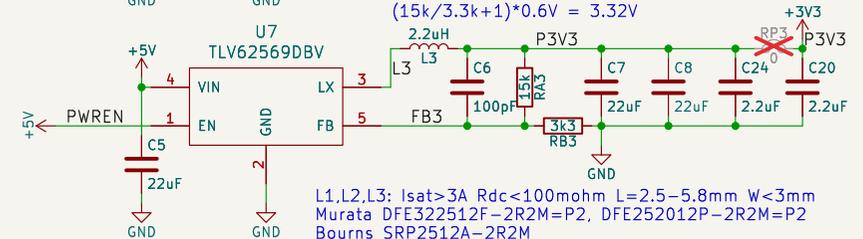
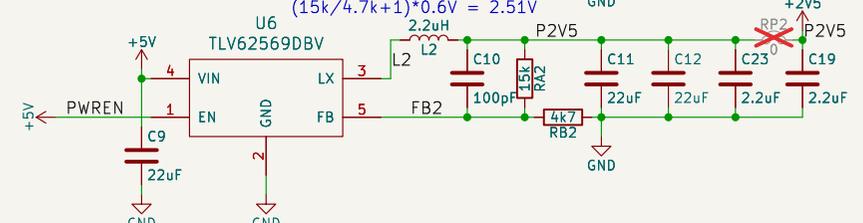
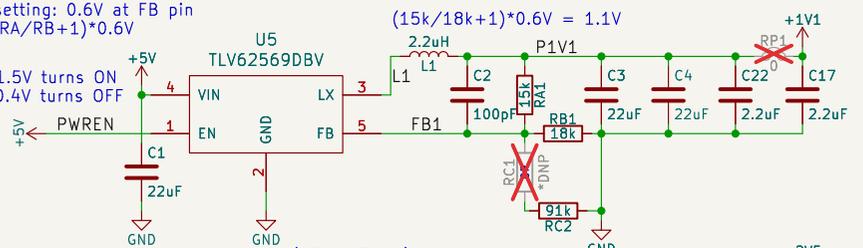
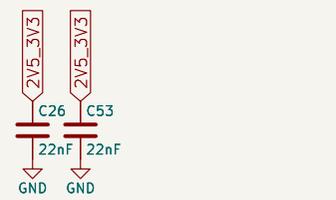
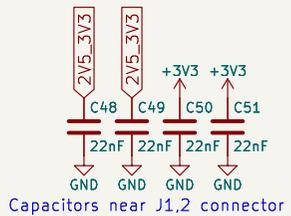
voltage setting: 0.6V at FB pin
 $V_{out} = (RA/RB+1)*0.6V$
PWREN
above +1.5V turns ON
below +0.4V turns OFF



WARNING
ECP5 family datasheet
p.48: Power Supply Ramp rates
for all supplies 0.01-10V/ms

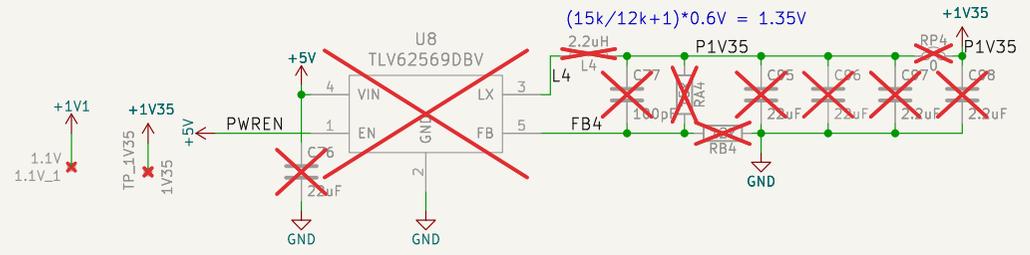
D11 (2V), R2, R4 hold PWREN on 1V
in the middle of 0.4-1.5V hysteresis

$C56 * C57 / (C56 + C57) + 4.5pF = 6pF$
 $4.5pF = 3pF \text{ chip} + 1pF \text{ crystal} + 0.5pF \text{ PCB}$



L1,L2,L3: Isat>3A Rdc<100mohm L=2.5-5.8mm W<3mm
Murata DFE322512F-2R2M=P2, DFE252012P-2R2M=P2
Bourns SRP2512A-2R2M

Switching regulators 2A SOT23-5
Texas instruments TLV62569DBV (2A) (best)
Dioo microcircuits DI06015B (1.5A) (osc. acceptable)
Microsemi LX7172 (1.2A) (osc. unacceptable)
Diodes AP3429/A (2A) - (will damage board)



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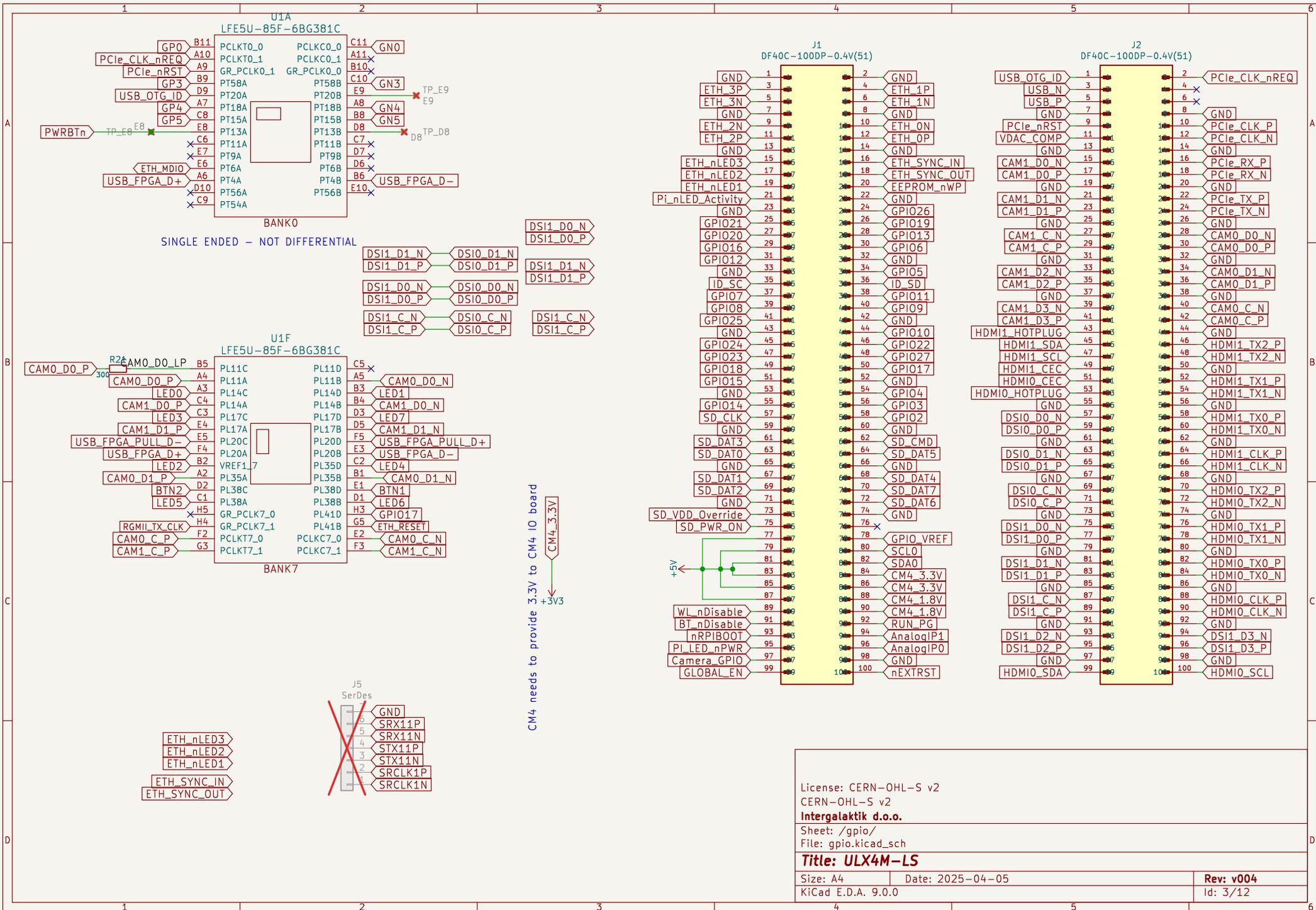
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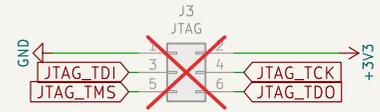
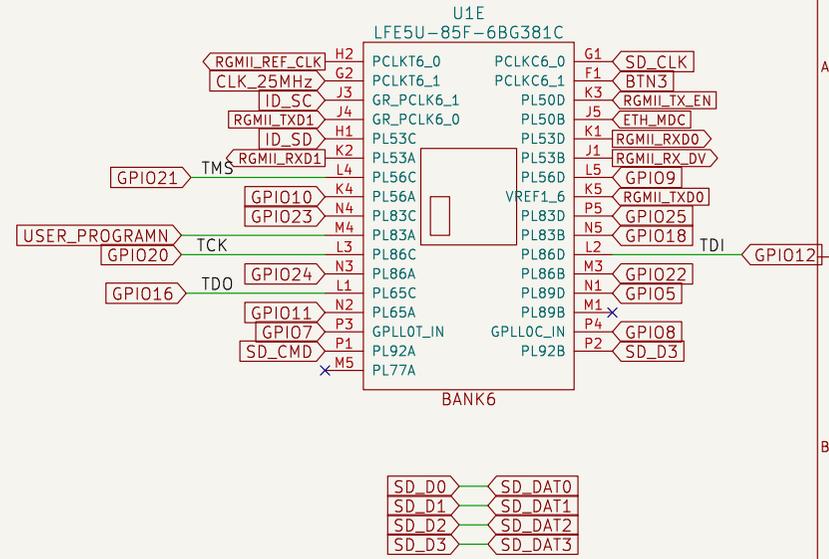
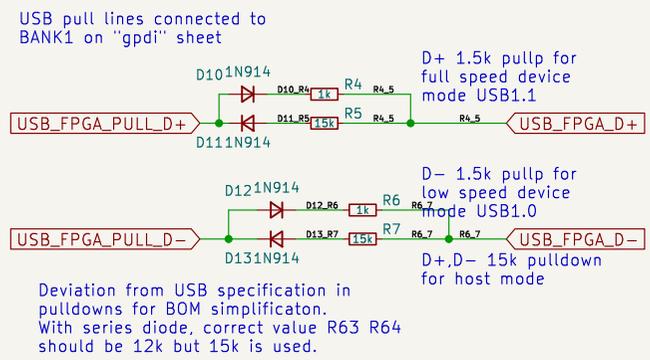
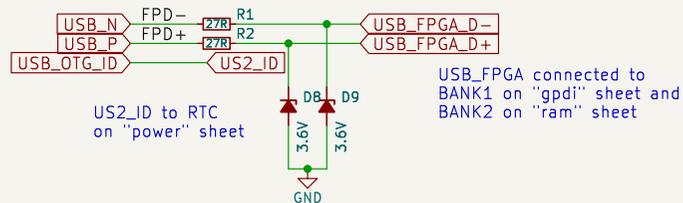
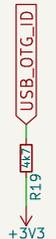
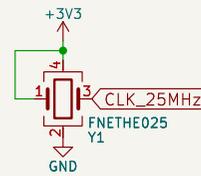
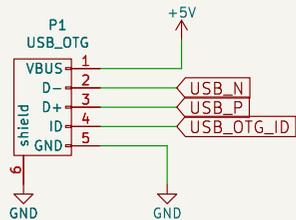
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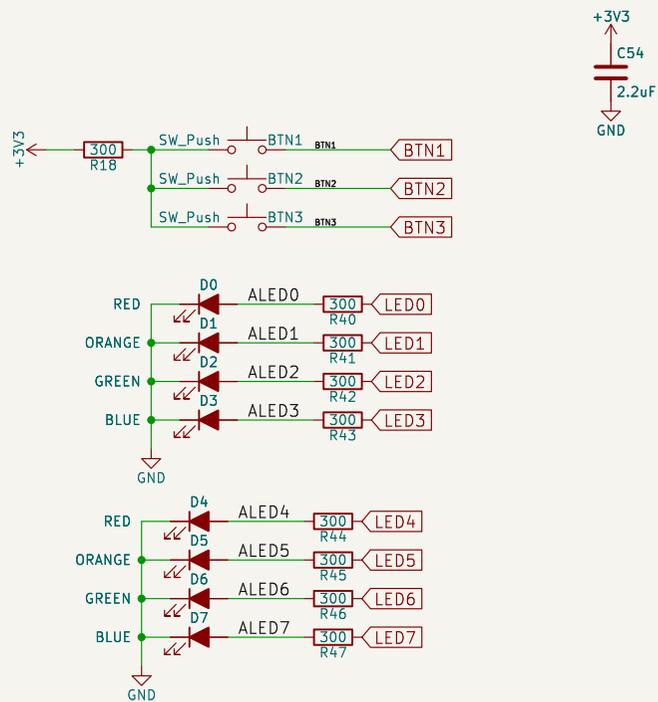
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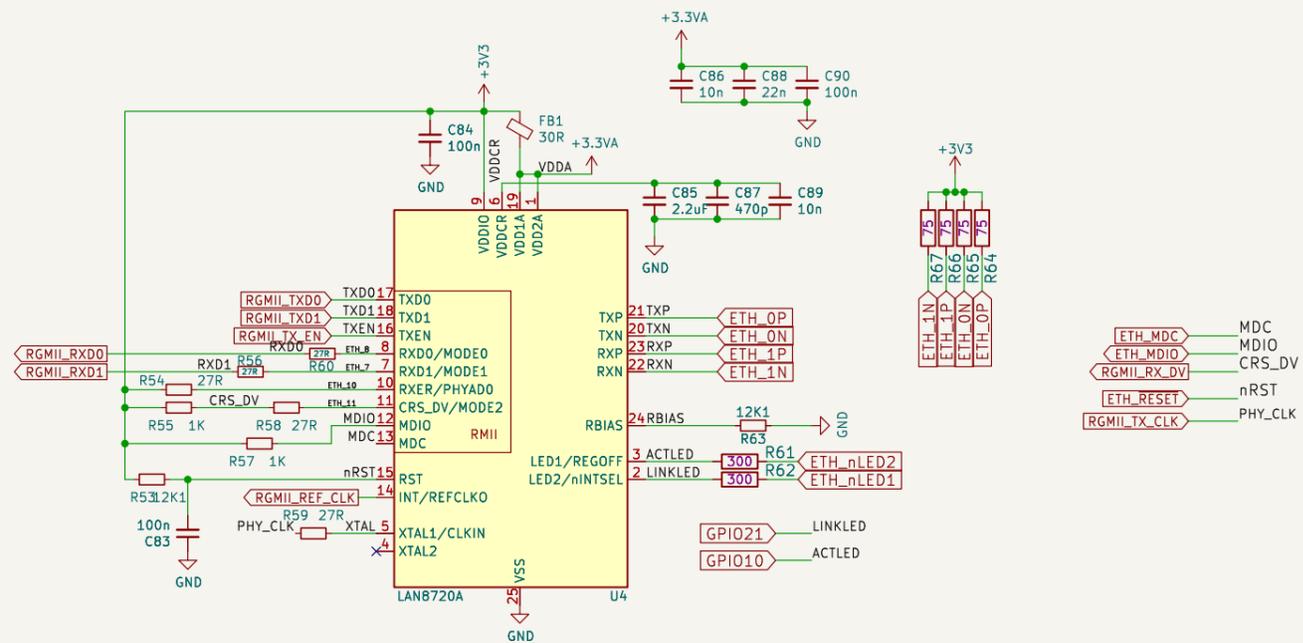
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Rev: v004

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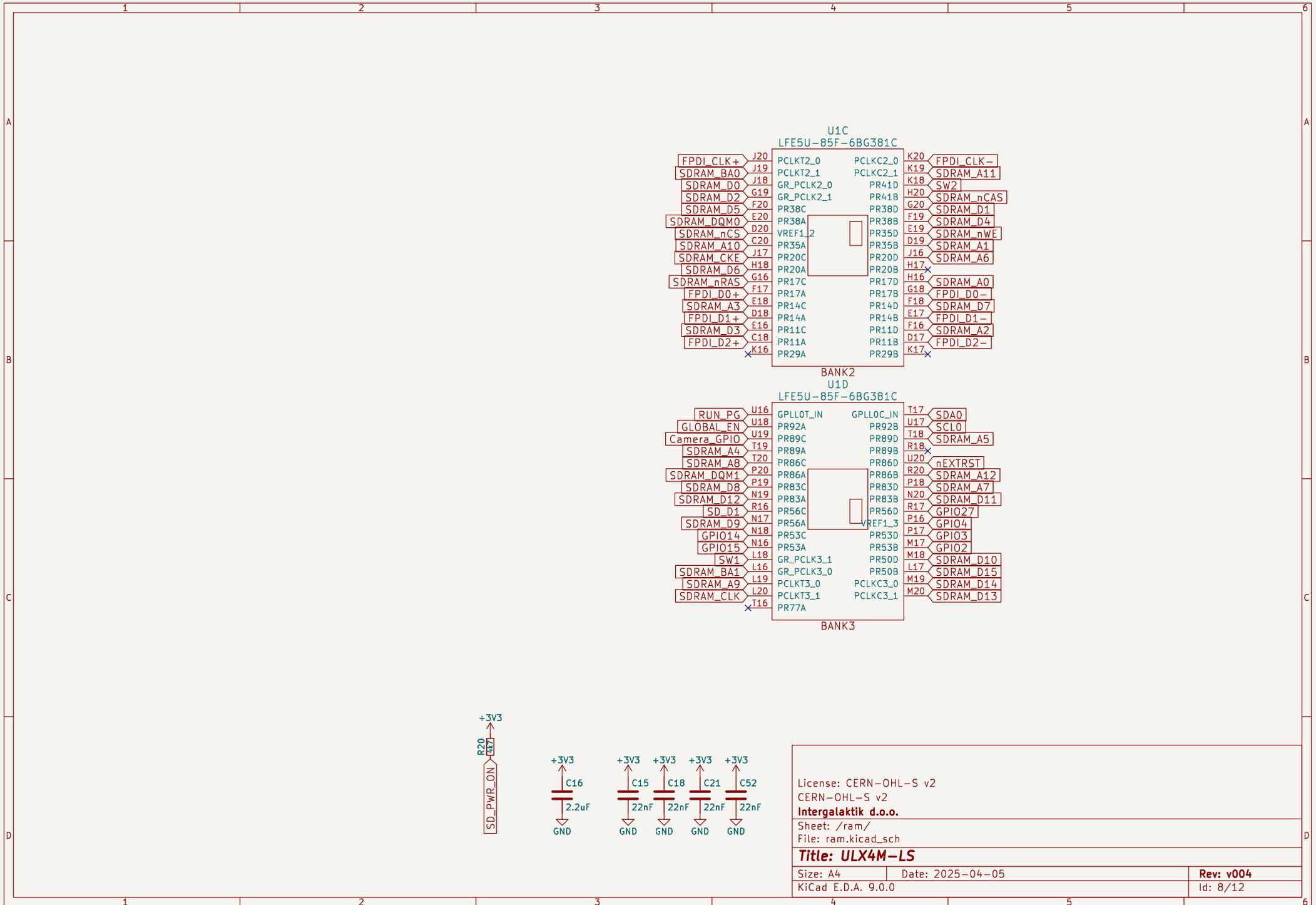
RJ45 connector

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Rev: v004
 Id: 7/12

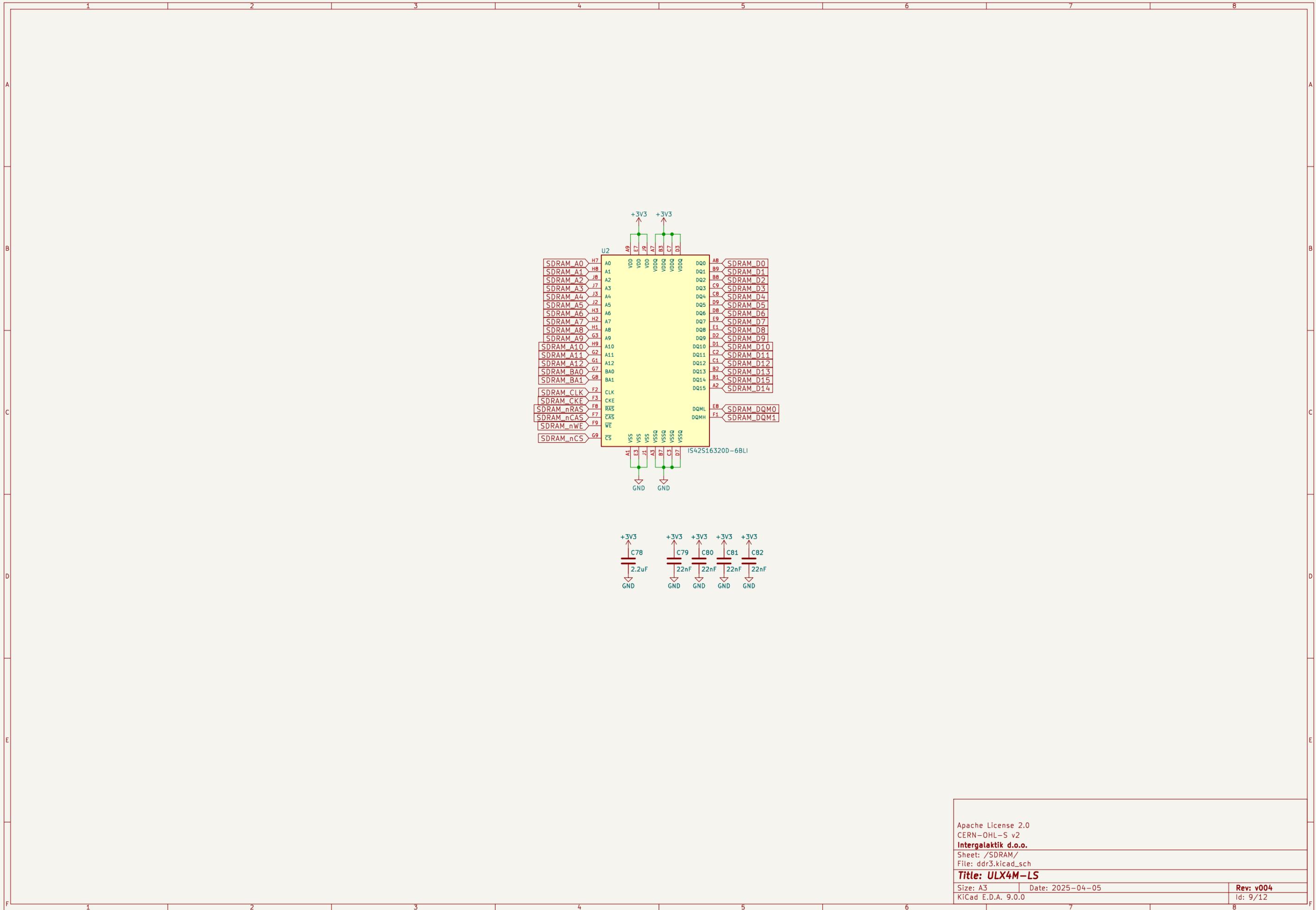


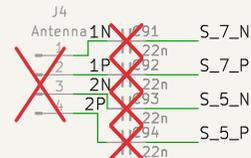
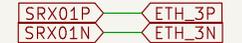
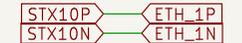
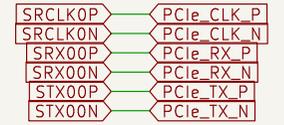
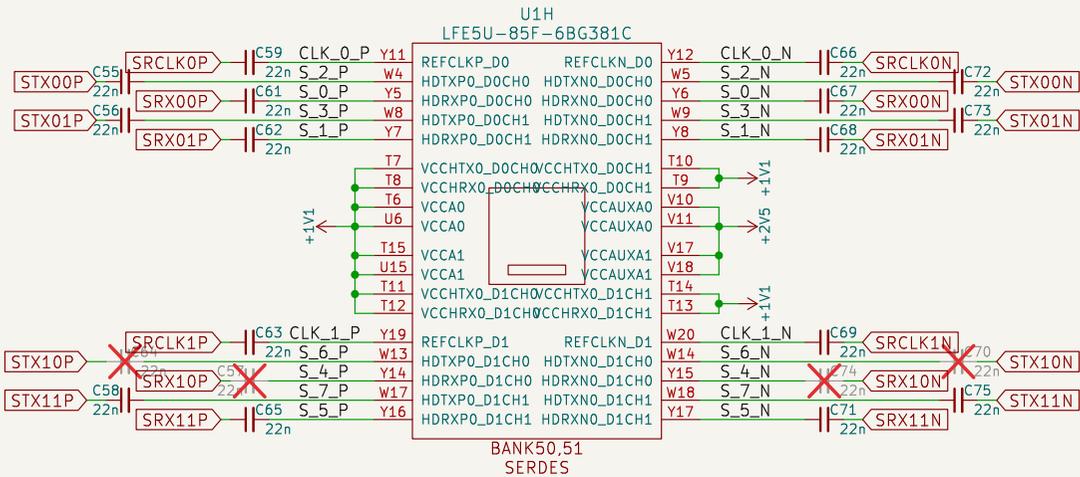
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Place shorts or caps for external antenna experiments

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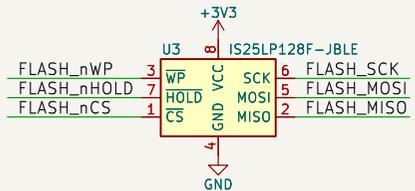
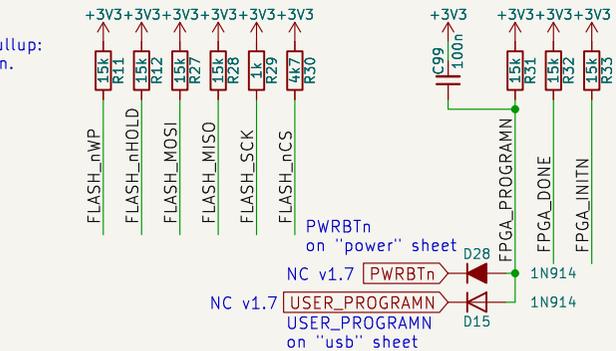
Rev: v004

Id: 10/12

Deviation from TN1260 in pullup: values for BOM simplification. Correct values should be 1k but 1.1k is used.

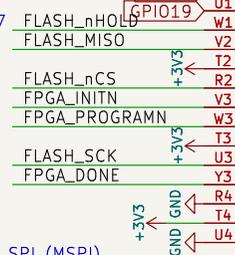
pullups for Master SPI (MSPI) required by TN1260: lattice ECP5 sysCONFIG guide p.6

pullups to allow entering USER mode TN1260: lattice ECP5 sysCONFIG guide p.6, p.8, p.13

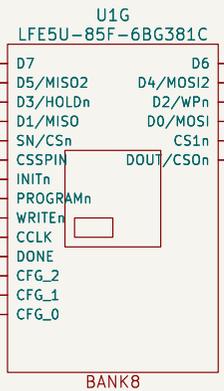


For programming Flash thru JTAG see Lattice FPGA-TN-02050

BTN_U v1.7



CFG select Master SPI (MSPI) TN1260: lattice ECP5 sysCONFIG guide p.17



BTN_R v1.7



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	1	2	3	4	5	6
A						A
B						B
C						C
D						D
	1	2	3	4	5	6

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Size: A4 Date: 2025-04-05

Rev: v004

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