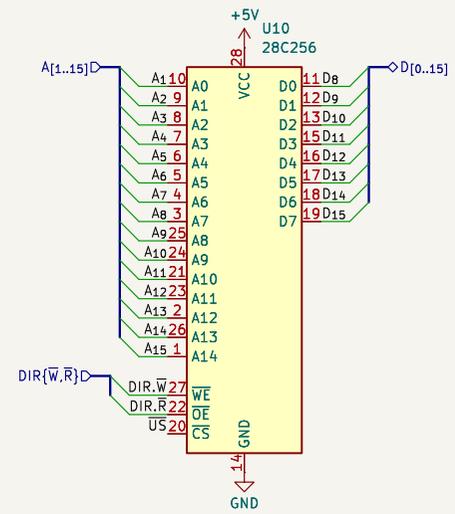
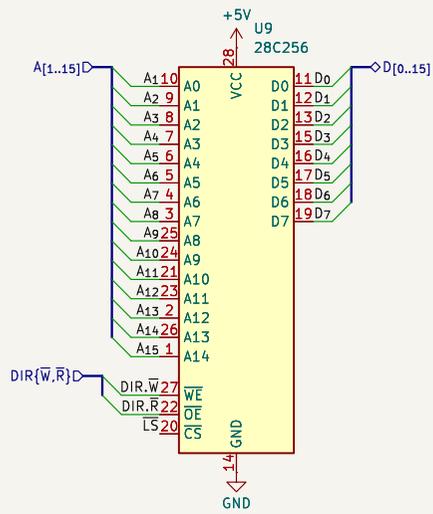
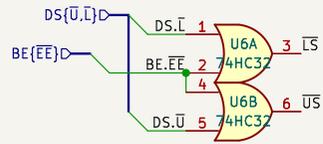


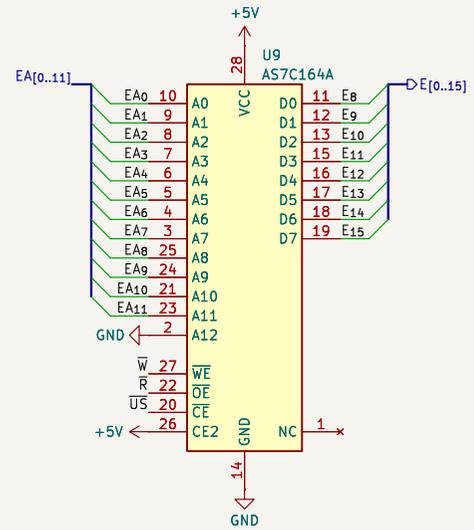
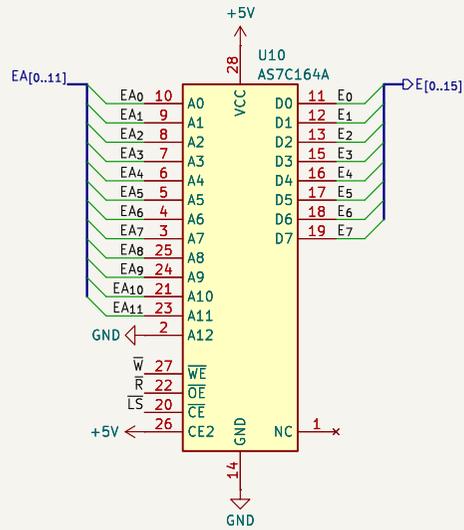
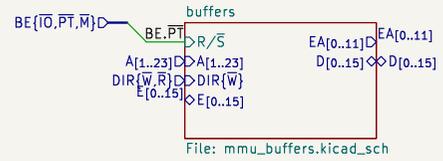
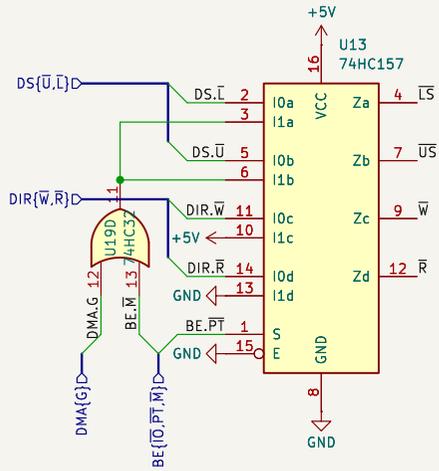
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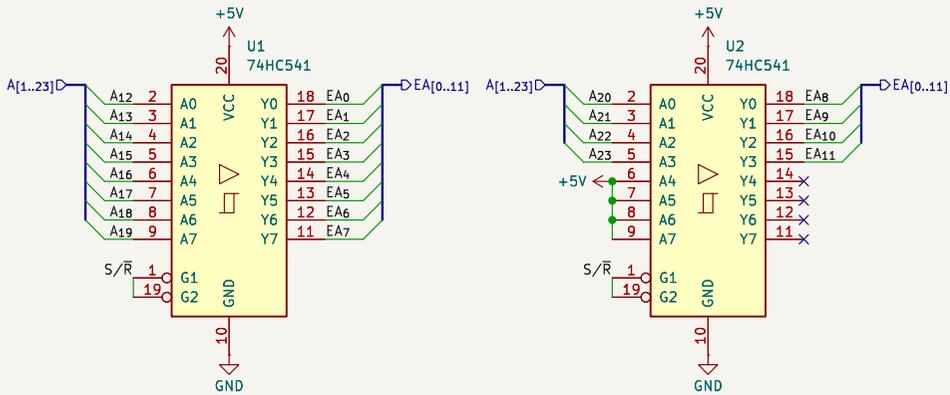
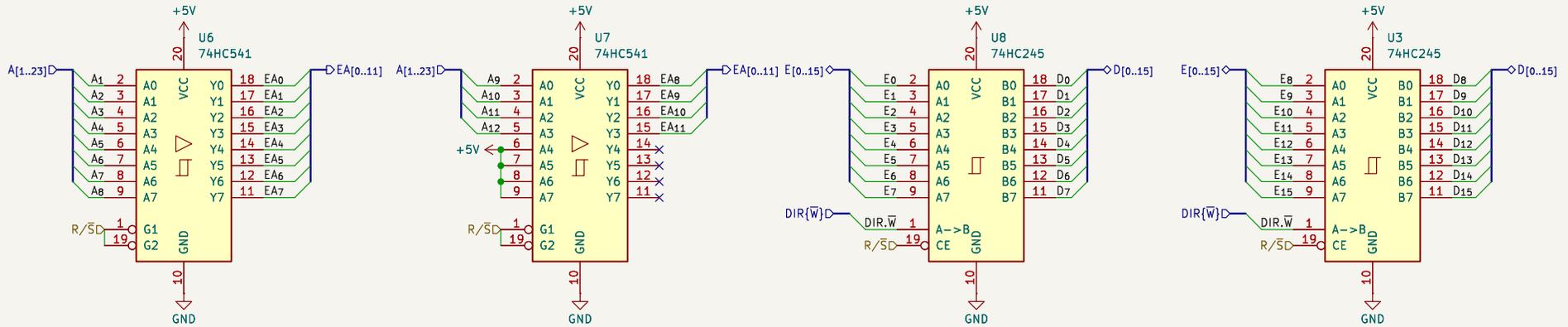
/BE.I = !(/AC.P & /AC.D)
/sas = eq8(A16-23, 0, /AC.S + /BE.I + !/BR.G)
/BE.IO = eq8(A8-15, 11011111, /sas)
/BE.PT = eq8(A13-15, 111, /sas)
/BE.EE = /sas + /io & /pt
/BE.M = /BE.I + /sas

```

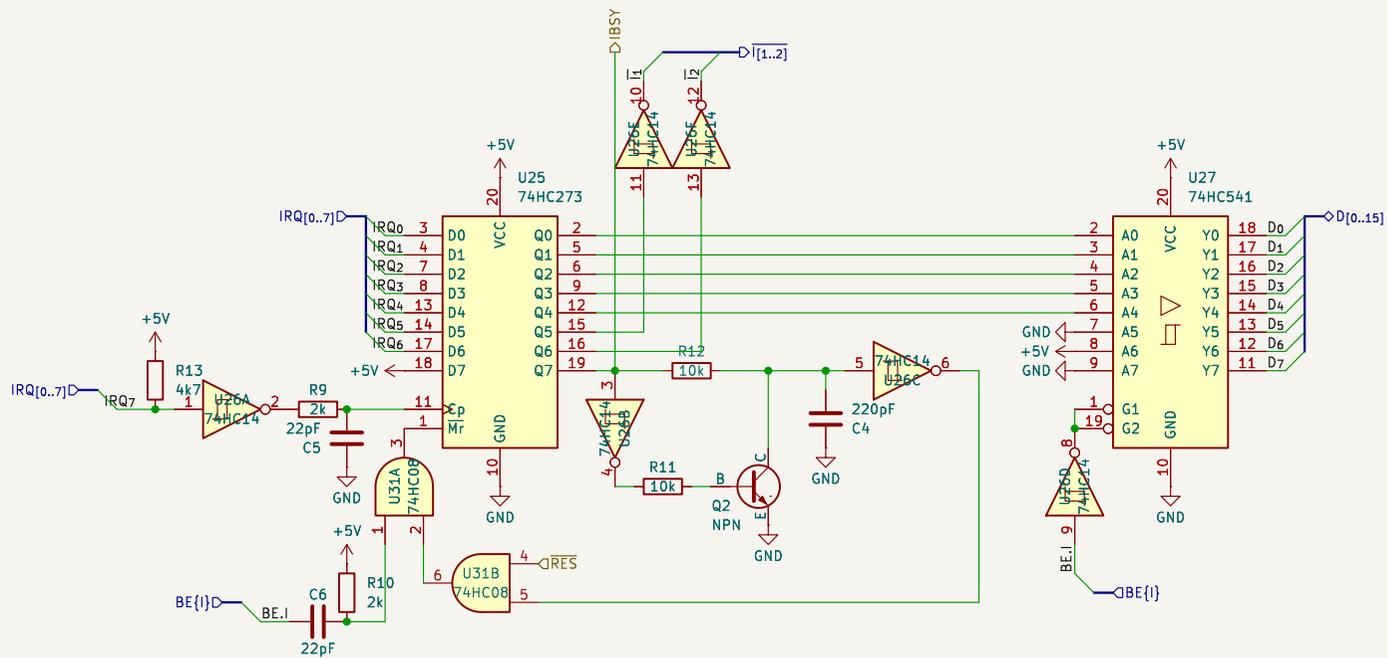


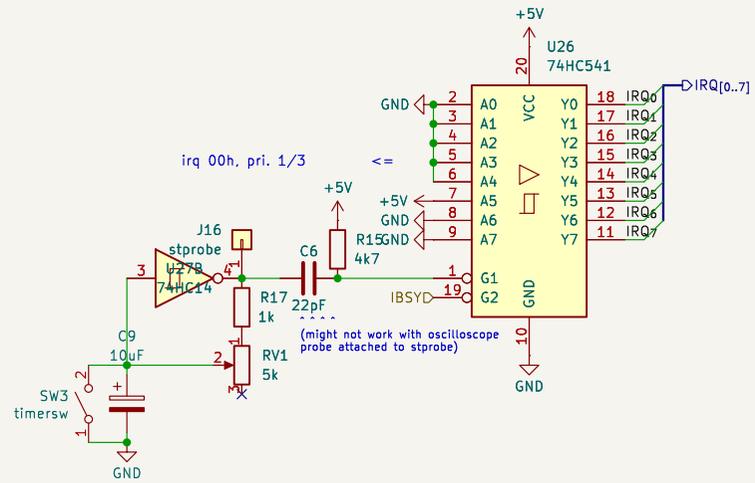
- modes:
- Ready ($BE.PT = 1$): the buses are set to address the PT ram to Abus's page and to export the output entry.
 - Set ($BE.PT = 0$): the buses are set to access the PT ram as normal ram.





no need to buffer Ebus before the output during the Ready mode.





what to control as a DMA bus master:

- $\overline{\text{DMA}}(\overline{\text{R}}, \overline{\text{SAS}})$ (obviously)
- $\text{A}[1..23]$ ($\text{A}[1..11] + \text{E}[0..11]$)
- $\text{D}[0..15]$
- $\text{DS}[\text{U}, \text{L}]$
- $\text{DIR}[\text{W}, \text{R}]$
- $\text{AC}[\text{P}, \text{D}, \text{U}]$
- ($\text{E}[13..15]$) (mmu flags, optional, pulled down)

