

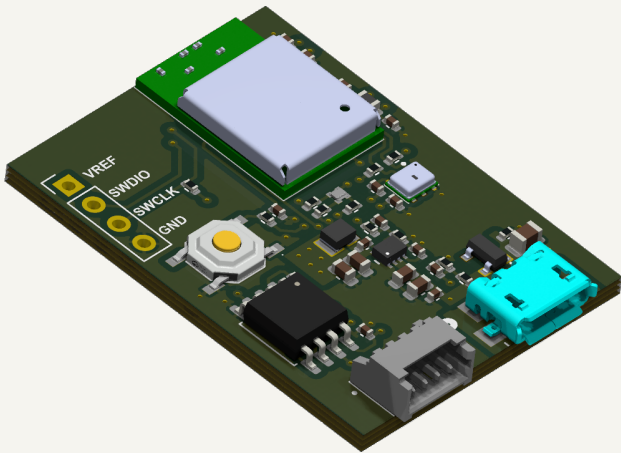
PCB NINA PROJECT

Variant: CHECKED

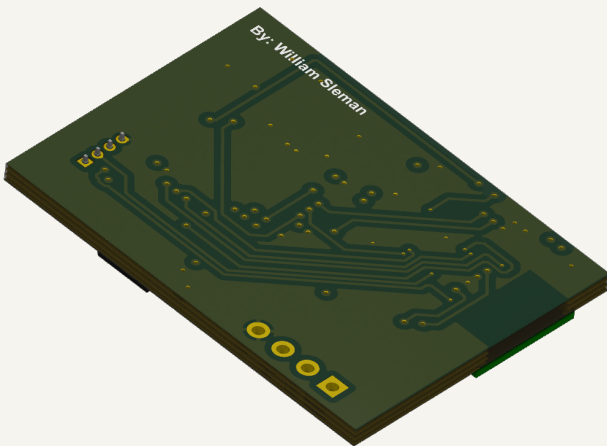
2026-02-13
Rev 1.0

Page	Index	Page	Index	Page	Index	Page	Index
1	Cover Page	11		21		31	
2	Block Diagram	12		22		32	
3	Power Supply	13		23		33	
4	MCU	14		24		34	
5	Revision History	15		25		35	
6		16		26		36	
7		17		27		37	
8		18		28		38	
9		19		29		39	
10		20		30		40	

TOP VIEW



BOTTOM VIEW



NOTES

Not fitted components are marked as **X**

DRAFT - Very early stage of schematic, ignore details.
PRELIMINARY - Close to final schematic.
CHECKED - There shouldn't be any mistakes. Contact the engineer if you find any.
RELEASED - A board with this schematic has been sent to production.

CHECKED 06-JAN-2026

DESIGN CONSIDERATIONS

DESIGN NOTE:

Example text for informational design notes.

DESIGN NOTE:

Example text for debug notes.

DESIGN NOTE:

Example text for cautionary design notes.

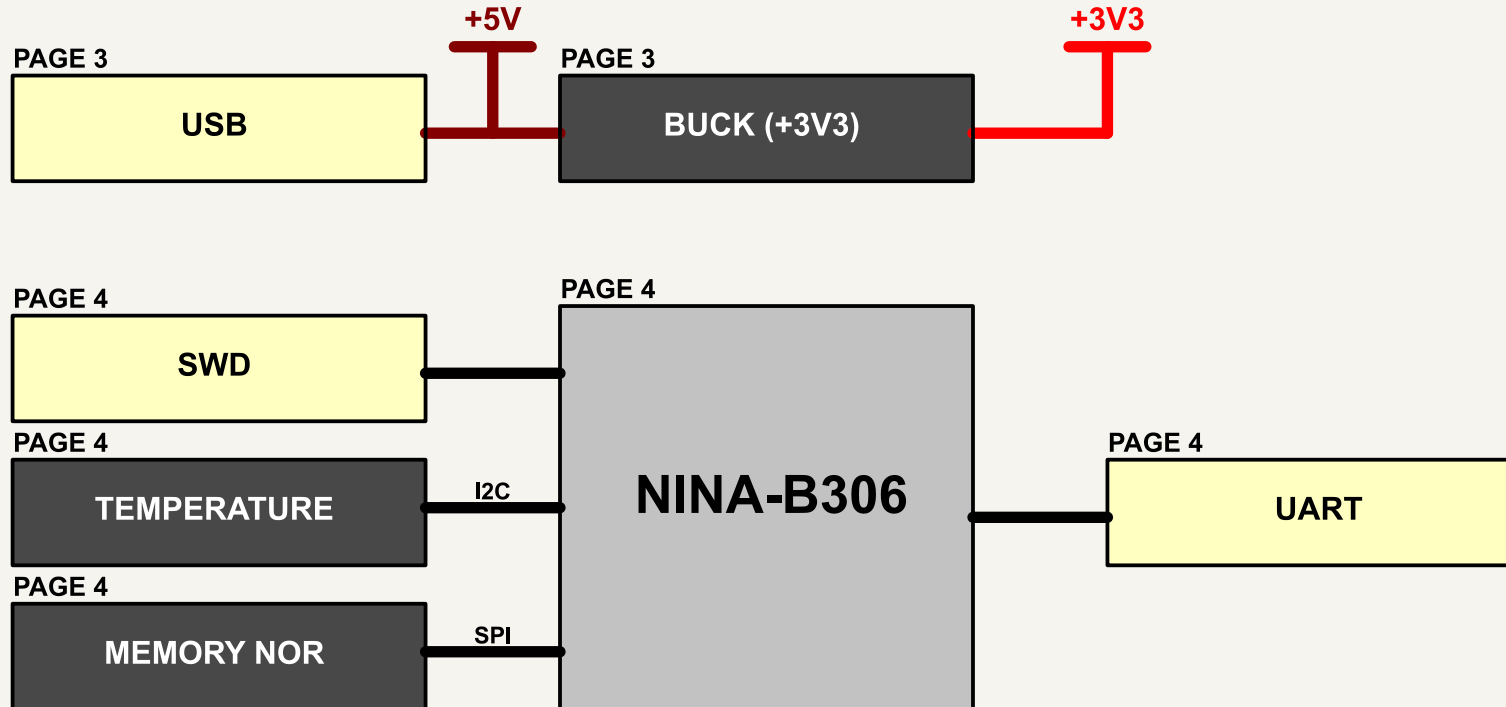
DESIGN NOTE:

Example text for critical design notes.

LAYOUT NOTE:

Example text for critical layout guidelines.

[02] - Block Diagram



Author: William Sleman

Sheet: /[02] - Block Diagram/

File: sheet2.kicad_sch

Title: PCB NRF52 PROJECT

Size: A4

Date: 2025-05-16

Rev: 1.0

KiCad E.D.A. 9.0.0

Id: 2/5

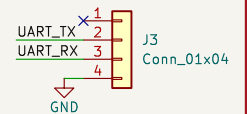
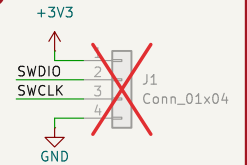
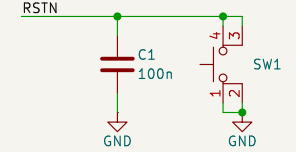
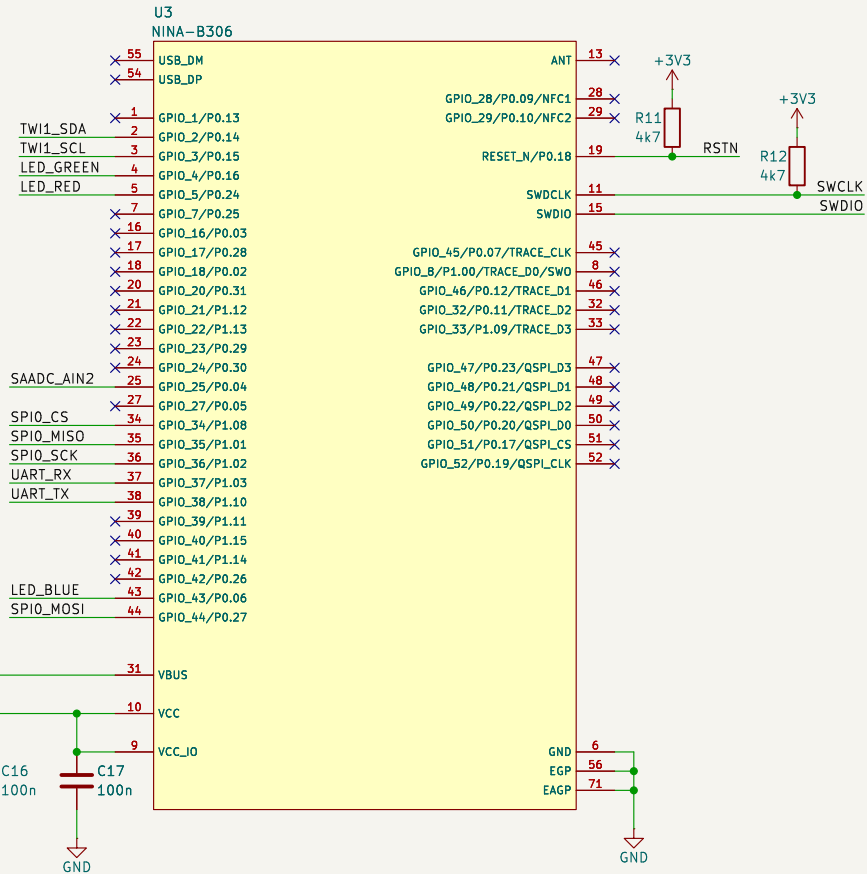
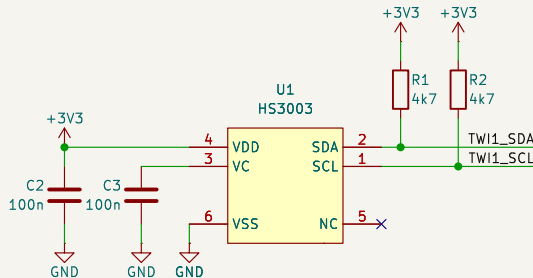
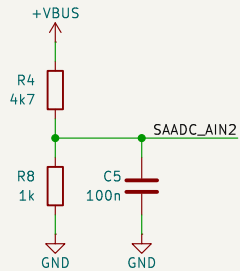
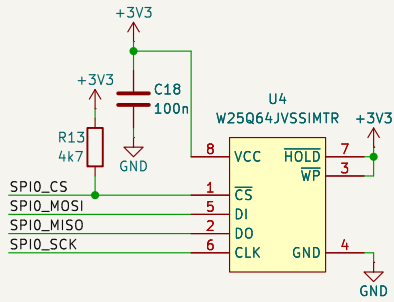
CONNECTOR



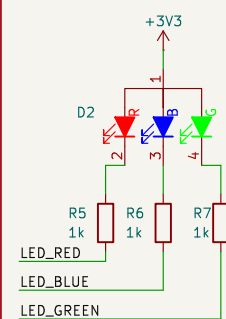
The schematic diagram illustrates the MP2322GQH-P buck converter circuit. The input is +VBUS, which is connected to the IN pin (pin 2) of the converter. The EN pin (pin 3) is connected to +VBUS through a 100nF capacitor (C7). The PG pin (pin 6) is connected to GND through a 10uF capacitor (C8). The VCC pin (pin 4) is connected to GND through a 10uF capacitor (C9). The GND pin (pin 1) is connected to GND through a 100nF capacitor (C13). The BST pin (pin 7) is connected to the SW pin (pin 8) through a 100nF capacitor (C6). The SW pin (pin 8) is connected to the output of the converter through an inductor (L1, MAKK2016T3R3M). The output is connected to the FB pin (pin 5) through a 976k resistor (R9) and a 22pF capacitor (C10). The output is also connected to the PWR_FLAG pin (pin 10) through a 10uF capacitor (C11) and a 220k resistor (R10). The output is connected to +3V3 through a 10uF capacitor (C12).

Id: 3/5

[04] - MCU



Use a FTDI module to interface.



Id: 4/5

[05] - Revision History

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Variant: xxx

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Author: William Sleman

Sheet: /[05] - Revision History/

File: sheet5.kicad_sch

Title: PCB NRF52 PROJECT

Size: A4

Date: 2025-05-16

Rev: 1.0

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Id: 5/5