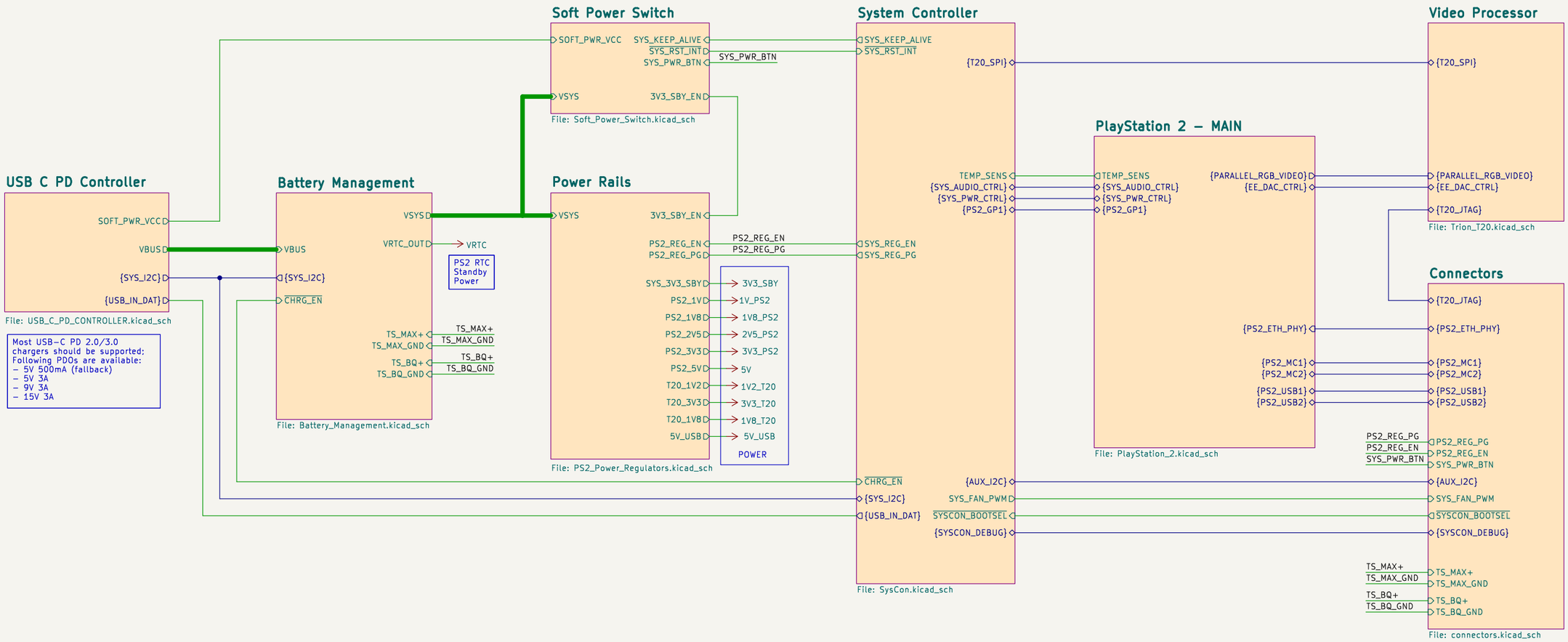
Custom PS2 Mainboard Top Level Schematics



Design Notes

Following components must be salvaged from a SCPH-7900x or SCPH-9000x mainboard:
- CXD2976GB (Emotion Engine)
- CXD2980 (Graphics Synthesizer)
- CXR726080 (MechaCon)
- CXD3098AQ (DSP)
- BCM5241 (Ethernet PHY)
- 627G04LF (Main Clock PLL)

Following components must be salvaged from a SCPH-7900x or earlier PS2 Slim revisions:
- USB A socket (DO NOT USE ONE FROM SCPH-9000x!!)

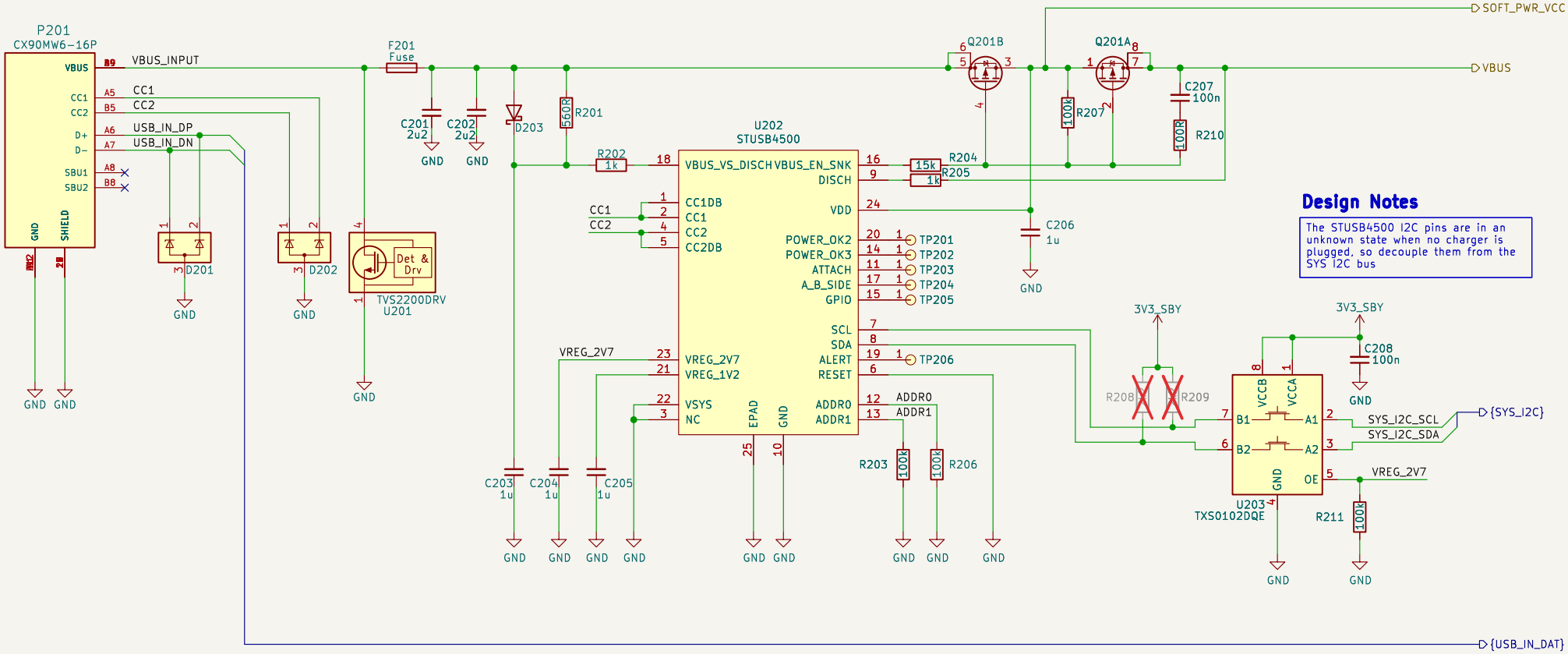
All remaining components can be purchased as specified in the BOM

This project would not exist without the bitbuilt.net community!
Special thanks to Mister M and Gman for their PS2 scans
and to Epaminondas for his work on the custom PS2 BIOS!

Sheet: /
File: PS2_79004_Rev_0_4.kicad_sch

Title: PS2 AIO Mainboard

Size: A3	Date:	**Rev: 0.3**
KiCad E.D.A. 9.0.0		Id: 1/30



Sheet: /USB C PD Controller/		
File: USB_C_PD_CONTROLLER.kicad_sch		
Title: PS2 USB C Input		
Size: A4	Date:	**Rev: 0.3**
KiCad E.D.A. 9.0.0		Id: 2/30

Battery Management

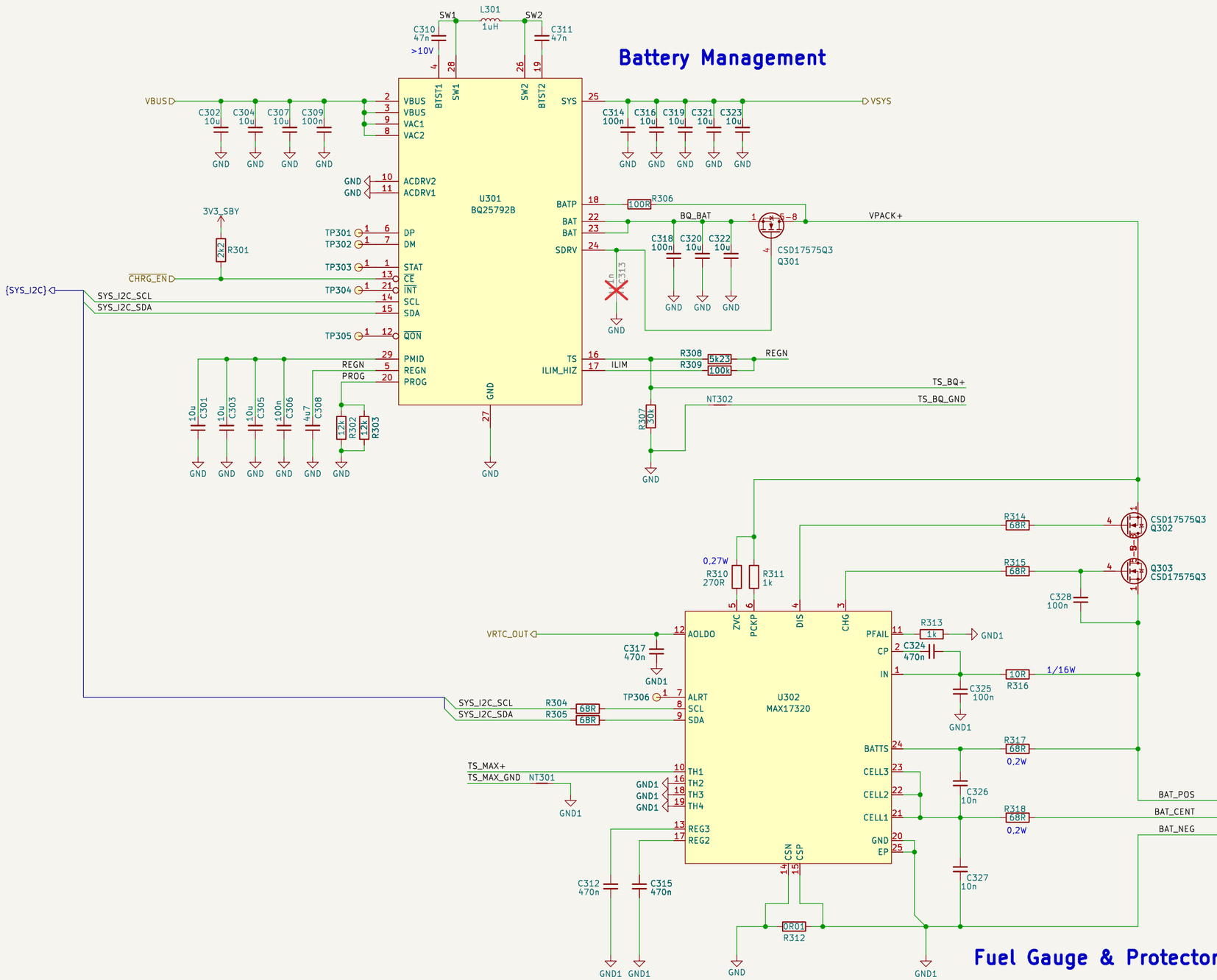
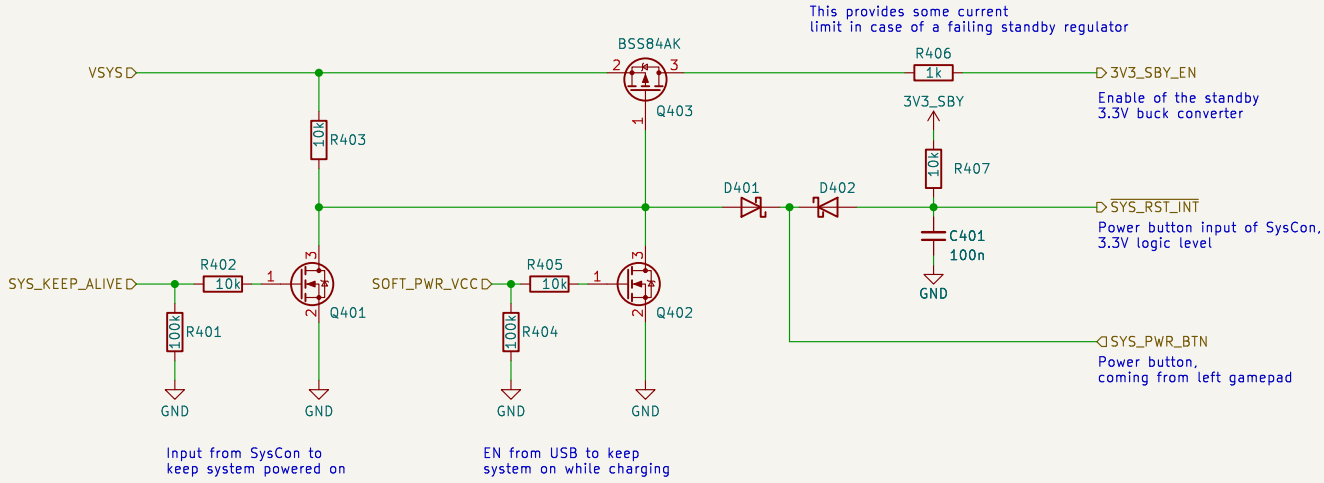


Table 53. Current Measurement Range and Resolution vs. Sense Resistor Value

BATTERY FULL CAPACITY (mAh)	SENSE RESISTOR (mΩ)	nRSENSE	CURRENT REGISTER RESOLUTION (µA)	CURRENT REGISTER RANGE (A)	CAPACITY RESOLUTION (mAh)	MAXIMUM CAPACITY (mAh)
> 4000	1	0064h	1562.5	±51.2	5	144360
> 2000	2	00C8h	781.25	±25.6	2.5	71680
> 800	5	01F4h	312.5	±10.24	1	28672
> 400	10	03E8h	156.25	±5.12	0.5	14336
> 200	20	07D0h	78.125	±2.56	0.25	7168

Sheet: /Battery Management/		
File: Battery_Management.kicad_sch		
Title: PS2 BMIC and Fuel Gauge		
Size: A3	Date:	**Rev: 0.3**
KiCad E.D.A. 9.0.0		Id: 3/30



Sheet: /Soft Power Switch/		
File: Soft_Power_Switch.kicad_sch		
Title: PS2 Soft Power Switch		
Size: A4	Date:	**Rev: 0.3**
KiCad E.D.A. 9.0.0		Id: 4/30

VSYS
PS2_REG_PG
PS2_REG_EN

U502
TPS629210
C504 22u
C510 100n
L501 2u2
C516 100n
C521 22u
MODE_1V2
R502 42k2
GND sets 1.2V

ALTERNATIVE: EXLA1V0402-2R2-R
U503
TPS629210
C505 22u
C511 100n
L502 2u2
C517 100n
C522 22u
nc sets 3.3V
MODE_3V3
R503 42k2

U501
MPQ8626GD
C501 10u
C502 10u
C506 4u7
C509 4u7
C514 220n
L505 1u
R508 10k
C520 270p
C525 10n
C526 47u
C527 47u
1V25_FB
R509 15k
C503 4u7
R506 6k8
C515 22n

U504
TPS629210
C507 22u
C512 100n
L503 2u2
C518 100n
C523 22u
5V_VSET
R507 100k
sets 5.1V
MODE_5V
R504 42k2

U505
TPS629210
C508 22u
C513 100n
L504 2u2
C519 100n
C524 22u
nc sets 3.3V
3V3_SBY_EN
MODE_3V3_SBY
R501 10k
R505 42k2

JP501
JP502
JP503
JP504
JP505
JP506

Design Notes

Before closing Jumpers, measure and record the impedance to GND
Compare to impedance table

U509
TLV75518PDRV
C531 4u7
C538 4u7

U507
TLV75525PDRV
C529 4u7
C534 4u7

U508
TLV75518PDRV
C530 4u7
C535 4u7

U506
AP22653A
C528 4u7
PS2_REG_EN
PS2_REG_PG
R510 45k3
C532 100n
C533 22u
C536 22u
C537 22u

T20_1V2
T20_1V8
T20_3V3

PS2_3V3
PS2_2V5
PS2_1V8
PS2_1V
PS2_5V

5V_USB
SYS_3V3_SBY

FPGA Power Rails

PS2 Power Rails

Including Audio Amp

USB A Port Supply

SysCon Standby Supply

Sheet: /Power Rails/	
File: PS2_Power_Regulators.kicad_sch	
Title: PS2 Power	
Size: A3	Date:
KiCad E.D.A. 9.0.0	Rev: 0.3
	Id: 5/30

System Controller

2x ARM Cortex-M0+
@133MHz

Design Notes

Place the buffer on BOOTSEL close to the flash, for signal integrity;

The 2k2 pullup ensures that bootsel is not triggered when the gamepad is initializing/no gamepad is connected

Power Management
USB C PD Controller
Battery Management
SYS_I2C_SDA
SYS_I2C_SCL
{SYS_I2C}

Left Gamepad
Right Gamepad
AUX_I2C_SDA
AUX_I2C_SCL
{AUX_I2C}

Audio Codec
AUX_I2C_SDA
AUX_I2C_SCL
SYS_HP_SENSE
{SYS_AUDIO_CTRL}

Connection to
Gamepad 1 port of PS2
SYS_GP1_CLK
SYS_GP1_DAT
SYS_GP1_CMD
SYS_GP1_ATT
SYS_GP1_ACK
{PS2_GP1}

Power Control
and Supervision of PS2
PS2_RESET
PS2_LED_GREEN
PS2_LED_RED
{SYS_PWR_CTRL}

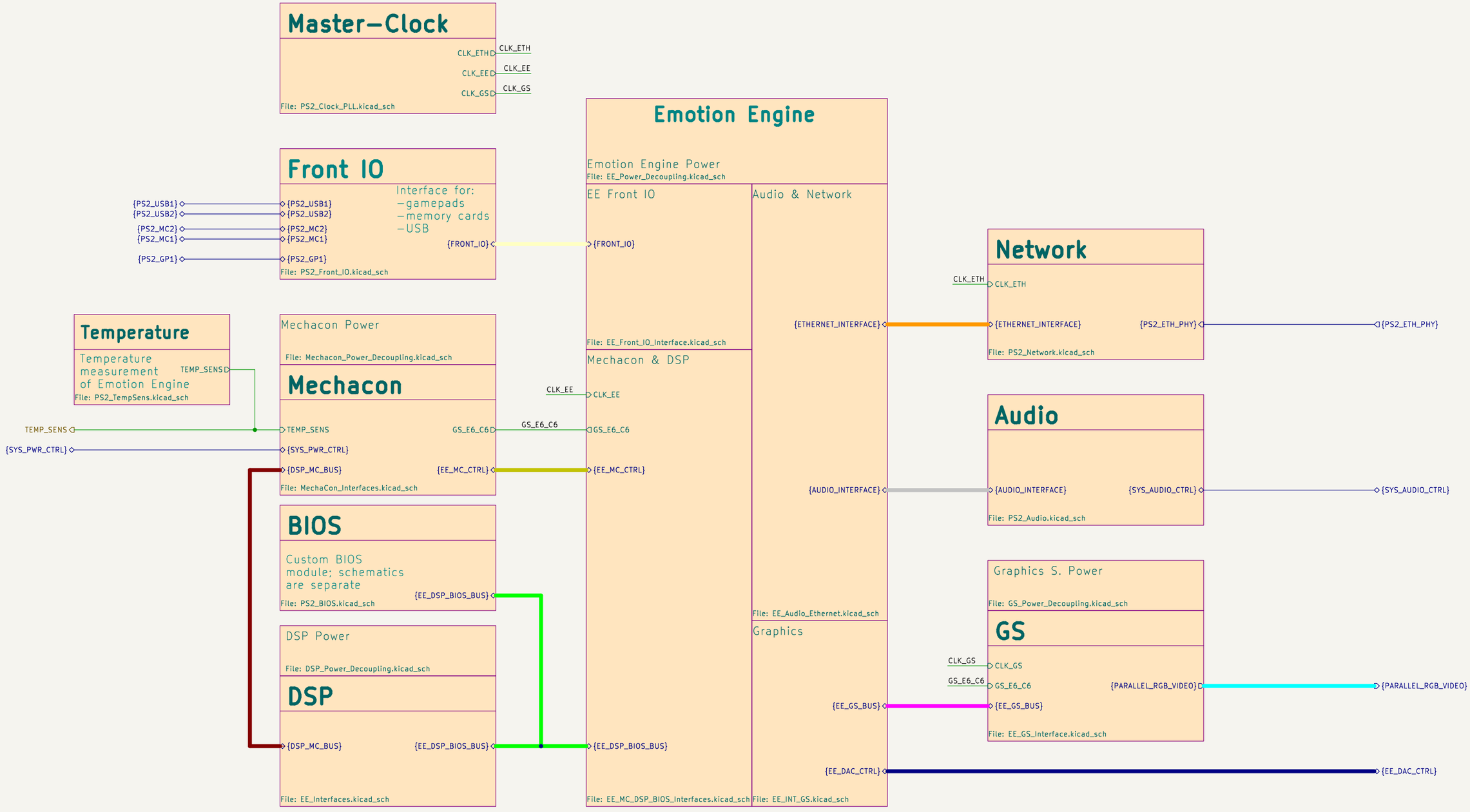
FPGA Configuration
and Communcation
T20_SPI_SCK
T20_SPI_TX
T20_SPI_RX
T20_SPI_CE0
T20_CRESET
T20_CDONE
T20_SPI_CE1
{T20_SPI}

USB to Type-C Connector
For SysCon FW Update
and debugging
USB_IN_DP
USB_IN_DN
{USB_IN_DAT}

Debug Interface for
SysCon
SYS_SWCLK
SYS_SWDIO
SYS_UART_TX
SYS_UART_RX
{SYSCON_DEBUG}

should be quite small to override RP2040 pulldowns during init

Sheet: /System Controller/	
File: SysCon.kicad_sch	
Title: PS2 SysCon	
Size: A3	Date:
KiCad E.D.A. 9.0.0	**Rev: 0.3**
	Id: 6/30

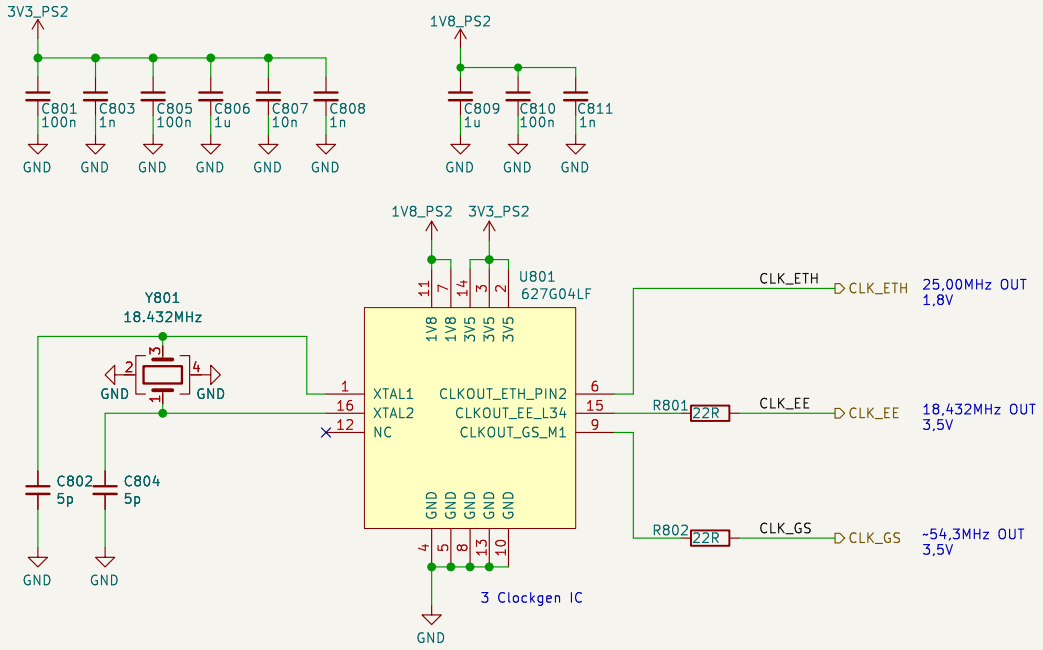


PS2 7900x – 9000x

Sheet: /PlayStation 2 – MAIN/
File: PlayStation_2.kicad_sch

Title: PS2 Top Level

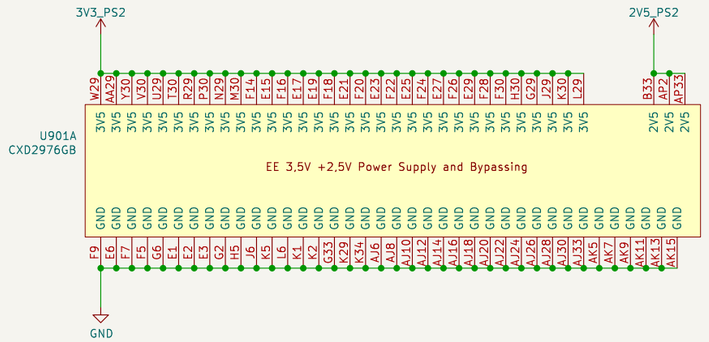
Size: A3	Date:	**Rev: 0.3**
KiCad E.D.A. 9.0.0		Id: 7/30

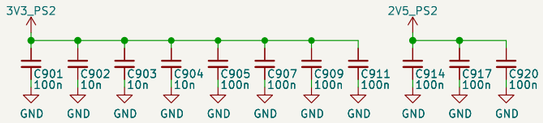


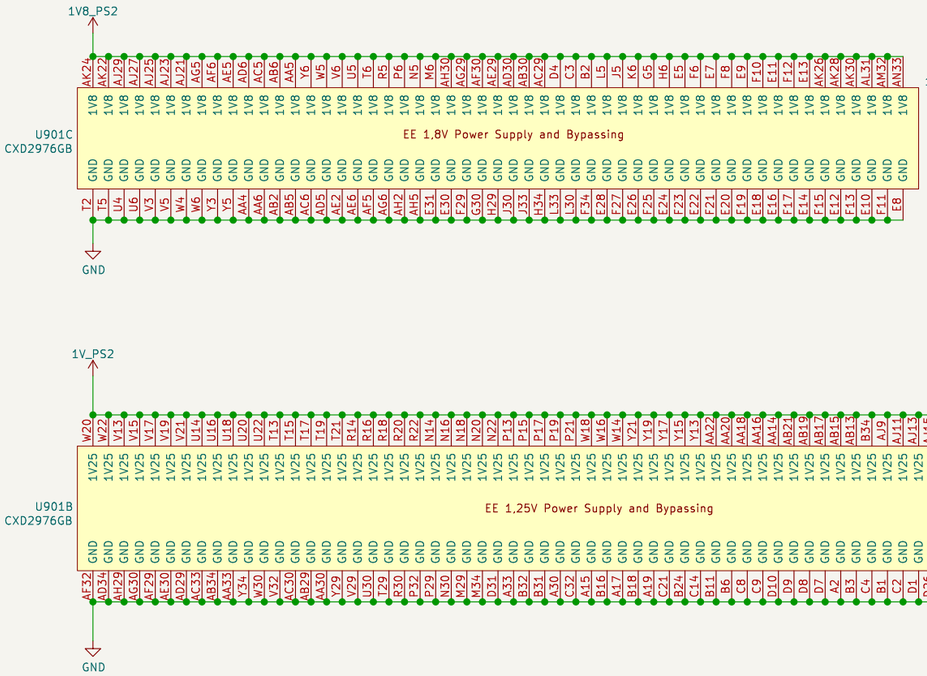
Sheet: /PlayStation 2 – MAIN/Master-Clock/
File: PS2_Clock_PLL.kicad_sch

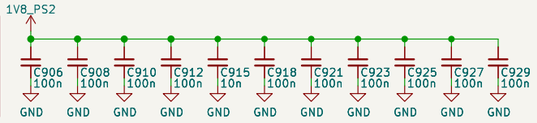
Title: PS2 Master Clock PLL

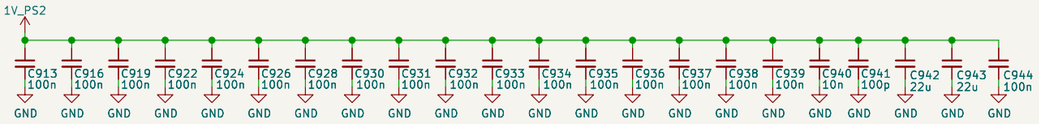
Size: A4	Date:	Rev: 0.3
KiCad E.D.A. 9.0.0		Id: 8/30







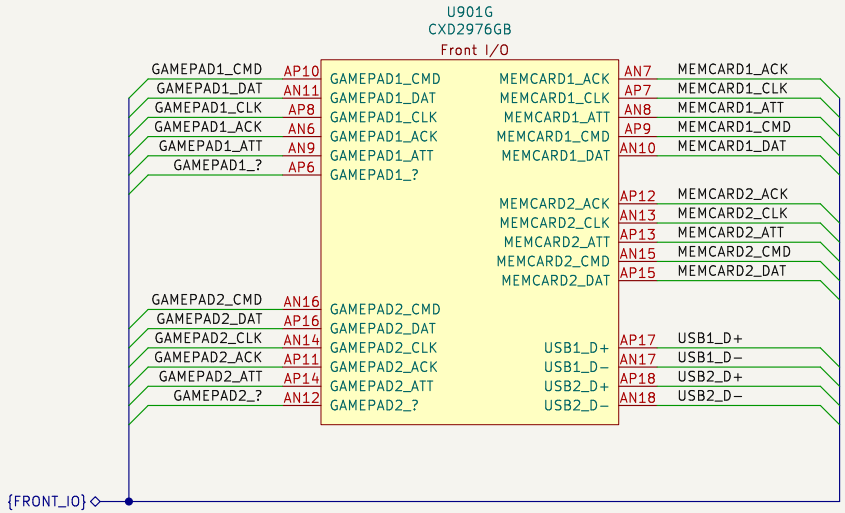




Sheet: /PlayStation 2 – MAIN/Emotion Engine Power/
File: EE_Power_Decoupling.kicad_sch

Title: PS2 Emotion Engine Power

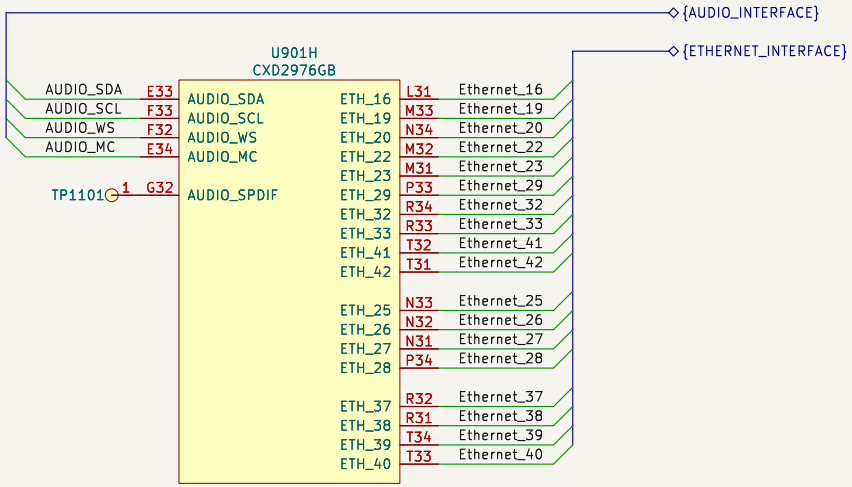
Size: A3	Date:	**Rev: 0.3**
KiCad E.D.A. 9.0.0		Id: 9/30



Sheet: /PlayStation 2 – MAIN/EE Front IO/
File: EE_Front_IO_Interface.kicad_sch

Title: PS2 Emotion Engine Front IO

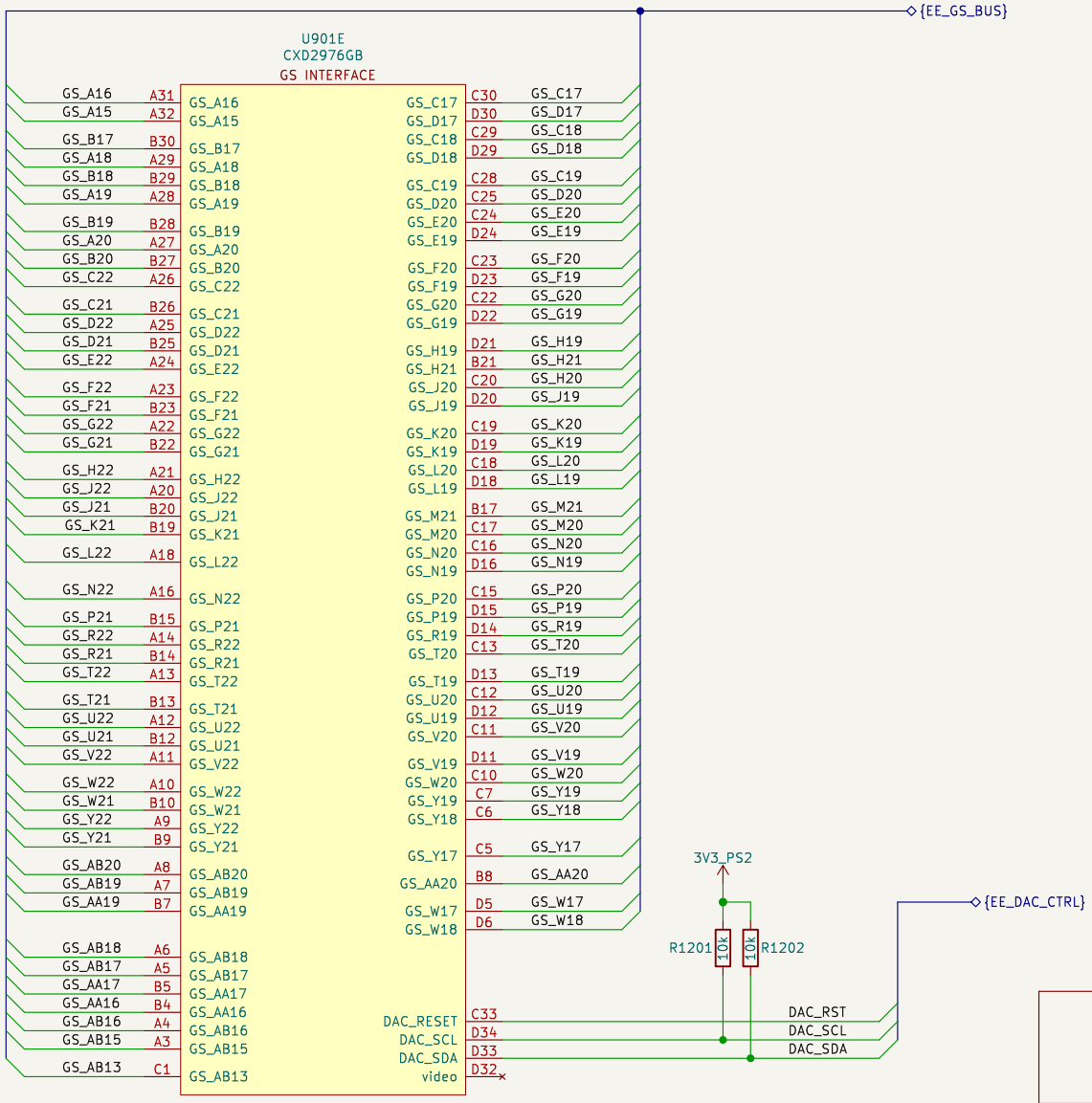
Size: A4	Date:	Rev: 0.3
KiCad E.D.A. 9.0.0		Id: 10/30



Sheet: /PlayStation 2 – MAIN/Audio & Network/
File: EE_Audio_Ethernet.kicad_sch

Title: PS2 Emotion Engine Audio & Network

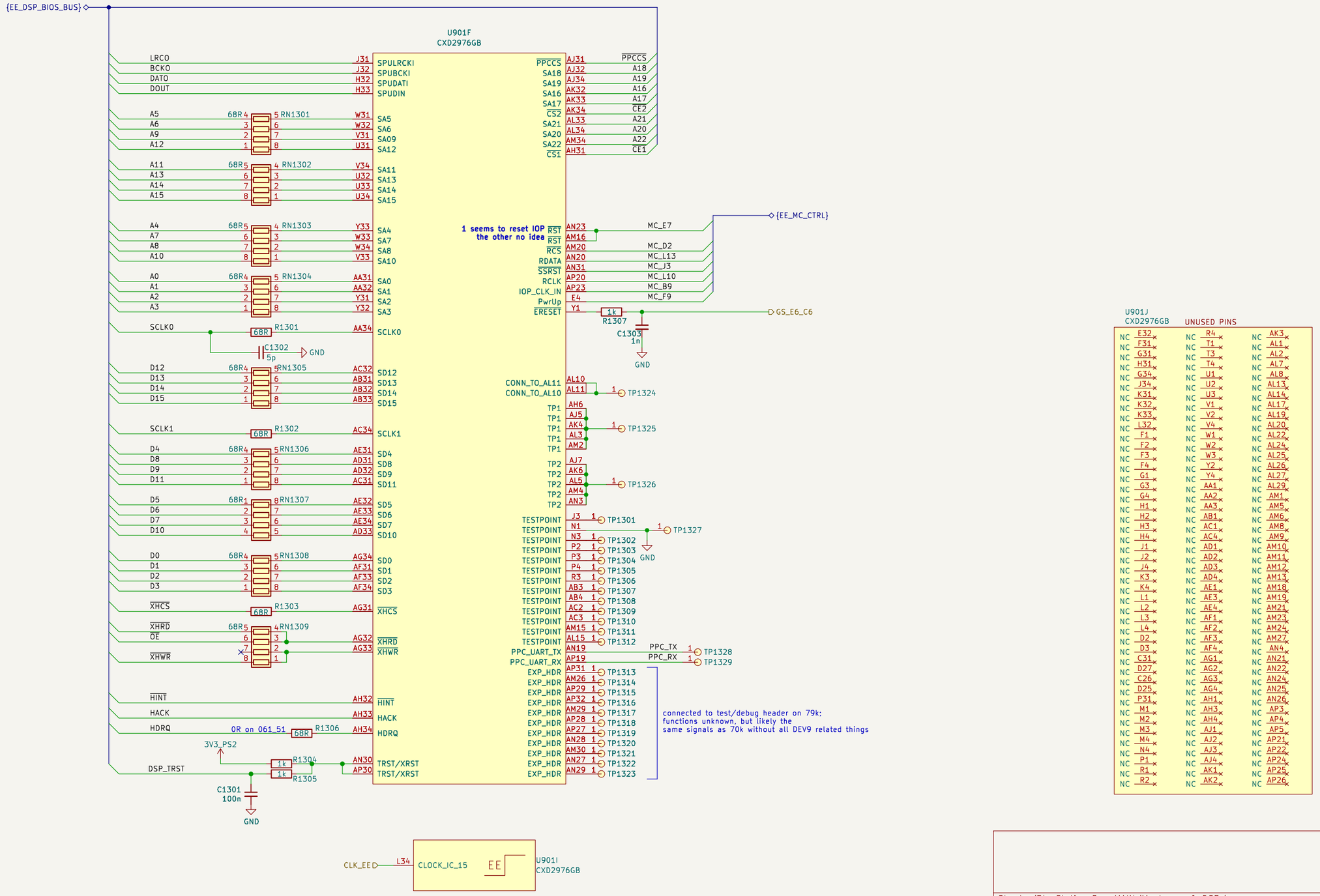
Size: A4	Date:	**Rev: 0.3**
KiCad E.D.A. 9.0.0		Id: 11/30

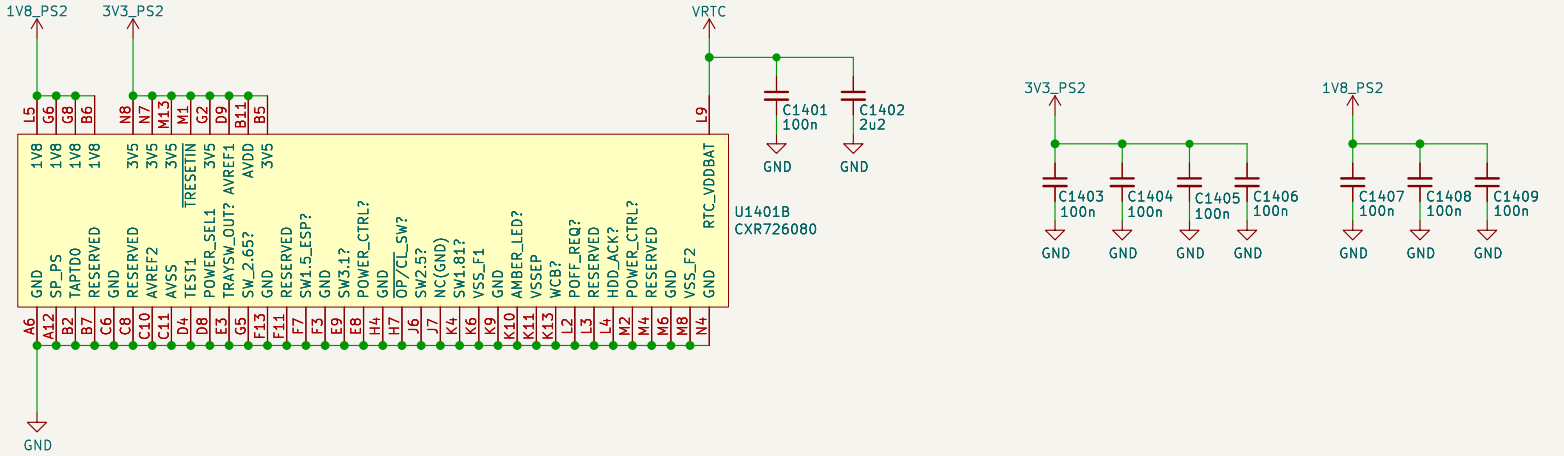


Sheet: /PlayStation 2 - MAIN/Graphics/
File: EE_INT_GS.kicad_sch

Title: PS2 EE - GS Interface

Size: A4	Date:	Rev: 0.3
KiCad E.D.A. 9.0.0		Id: 12/30


{EE_DSP_BIOS_BUS}
U901F
CXD2976GB
LRCO J31 SPULRCKI
BCKO J32 SPUBCKI
DATO H32 SPUDATI
DOUT H33 SPUDIN
A5 A6 A9 A12 68R RN1301 W31 W32 V31 U31 SA5 SA6 SA09 SA12
A11 A13 A14 A15 68R RN1302 V34 U32 U33 U34 SA11 SA13 SA14 SA15
A4 A7 A8 A10 68R RN1303 Y33 W33 W34 V33 SA4 SA7 SA8 SA10
A0 A1 A2 A3 68R RN1304 AA31 AA32 Y31 Y32 SA0 SA1 SA2 SA3
SCLK0 68R R1301 AA34 SCLK0
C1302 5p GND
D12 D13 D14 D15 68R RN1305 AC32 AB31 AB32 AB33 SD12 SD13 SD14 SD15
SCLK1 68R R1302 AC34 SCLK1
D4 D8 D9 D11 68R RN1306 AE31 AD31 AD32 AC31 SD4 SD8 SD9 SD11
D5 D6 D7 D10 68R RN1307 AE32 AE33 AE34 AD33 SD5 SD6 SD7 SD10
D0 D1 D2 D3 68R RN1308 AG34 AF31 AF33 AF34 SD0 SD1 SD2 SD3
XHCS 68R R1303 AG31 XHCS
XHRD OE 68R RN1309 AG32 AG33 XHRD XHWR
XHWR
HINT AH32 HINT
HACK AH33 HACK
HDRQ 0R on 061_51 68R R1306 AH34 HDRQ
3V3_PS2
DSP_TRST 1k R1304 1k R1305 AN30 AP30 TRST/XRST TRST/XRST
C1301 100n GND
PPCCS AJ31 PPCCS
SA18 AJ32 A18
SA19 AJ34 A19
SA16 AK32 A16
SA17 AK33 A17
CS2 AK34 CE2
SA21 AL33 A21
SA20 AL34 A20
SA22 AM34 A22
CS1 AH31 CE1
1 seems to reset IOP
the other no idea
RST AN23 MC_E7
RST AM16
RCS AM20 MC_D2
RDATA AN20 MC_L13
SSRST AN31 MC_J3
RCLK AP20 MC_L10
IOP_CLK_IN AP23 MC_B9
PwrUp E4 MC_F9
ERESET Y1 1k R1307 C1303 1n GND GS_E6_C6
{EE_MC_CTRL}
CONN_TO_AL11 AL10
CONN_TO_AL10 AL11 1 TP1324
TP1 AH6
TP1 AJ5
TP1 AK4 1 TP1325
TP1 AL3
TP1 AM2
TP2 AJ7
TP2 AK6
TP2 AL5 1 TP1326
TP2 AM4
TP2 AN3
TESTPOINT J3 1 TP1301
TESTPOINT N1 1 TP1327 GND
TESTPOINT N3 1 TP1302
TESTPOINT P2 1 TP1303
TESTPOINT P3 1 TP1304
TESTPOINT P4 1 TP1305
TESTPOINT R3 1 TP1306
TESTPOINT AB3 1 TP1307
TESTPOINT AB4 1 TP1308
TESTPOINT AC2 1 TP1309
TESTPOINT AC3 1 TP1310
TESTPOINT AM15 1 TP1311
TESTPOINT AL15 1 TP1312
PPC_UART_TX AN19 PPC_TX 1 TP1328
PPC_UART_RX AP19 PPC_RX 1 TP1329
EXP_HDR AP31 1 TP1313
EXP_HDR AM26 1 TP1314
EXP_HDR AP29 1 TP1315
EXP_HDR AP32 1 TP1316
EXP_HDR AM29 1 TP1317
EXP_HDR AP28 1 TP1318
EXP_HDR AP27 1 TP1319
EXP_HDR AN28 1 TP1320
EXP_HDR AM30 1 TP1321
EXP_HDR AN27 1 TP1322
EXP_HDR AN29 1 TP1323
connected to test/debug header on 79k;
functions unknown, but likely the
same signals as 70k without all DEV9 related things
U901J
CXD2976GB
UNUSED PINS
NC E32 NC F31 NC G31 NC H31 NC G34 NC J34 NC K31 NC K32 NC K33 NC L32 NC F1 NC F2 NC F3 NC F4 NC G1 NC G3 NC G4 NC H1 NC H2 NC H3 NC H4 NC J1 NC J2 NC J4 NC K3 NC K4 NC L1 NC L2 NC L3 NC L4 NC D2 NC D3 NC C31 NC D27 NC C26 NC D25 NC P31 NC M1 NC M2 NC M3 NC M4 NC N4 NC P1 NC R1 NC R2
NC R4 NC T1 NC T3 NC T4 NC U1 NC U2 NC U3 NC V1 NC V2 NC V4 NC W1 NC W2 NC W3 NC Y2 NC Y4 NC AA1 NC AA2 NC AA3 NC AB1 NC AC1 NC AC4 NC AD1 NC AD2 NC AD3 NC AD4 NC AE1 NC AE3 NC AE4 NC AF1 NC AF2 NC AF3 NC AF4 NC AG1 NC AG2 NC AG3 NC AG4 NC AH1 NC AH3 NC AH4 NC AJ1 NC AJ2 NC AJ3 NC AJ4 NC AK1 NC AK2
NC AK3 NC AL1 NC AL2 NC AL7 NC AL8 NC AL13 NC AL14 NC AL17 NC AL19 NC AL20 NC AL22 NC AL24 NC AL25 NC AL26 NC AL27 NC AL29 NC AM1 NC AM5 NC AM6 NC AM8 NC AM9 NC AM10 NC AM11 NC AM12 NC AM13 NC AM18 NC AM19 NC AM21 NC AM23 NC AM24 NC AM27 NC AN4 NC AN21 NC AN22 NC AN24 NC AN25 NC AN26 NC AP3 NC AP4 NC AP5 NC AP21 NC AP22 NC AP24 NC AP25 NC AP26
CLK_EED L34 CLOCK_IC_15 EE U901I CXD2976GB
Sheet: /PlayStation 2 – MAIN/Mechacon & DSP/
File: EE_MC_DSP_BIOS_Interfaces.kicad_sch
Title: PS2 EE – Mechacon – DSP Interface
Size: A3
Date:
Rev: 0.3
KiCad E.D.A. 9.0.0
Id: 13/30

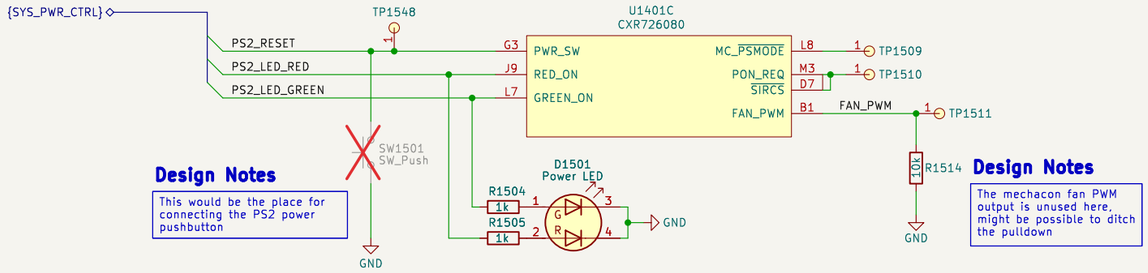


Sheet: /PlayStation 2 – MAIN/Mechacon Power/
File: Mechacon_Power_Decoupling.kicad_sch

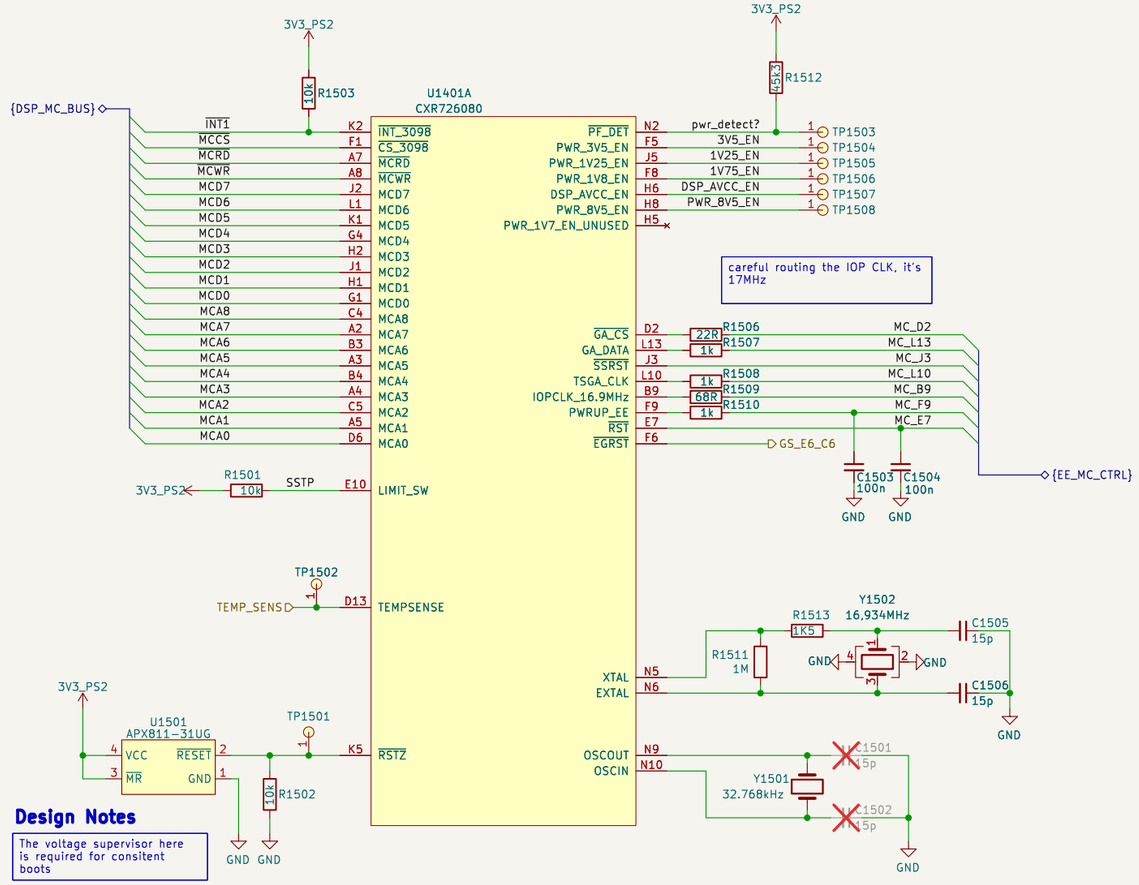
Title: PS2 Mechacon Power

Size: A4	Date:	**Rev: 0.3**
KiCad E.D.A. 9.0.0		Id: 14/30

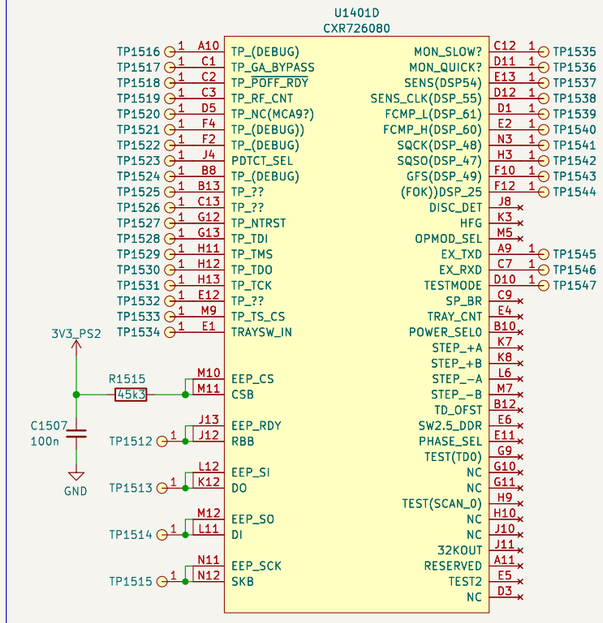
Power Control



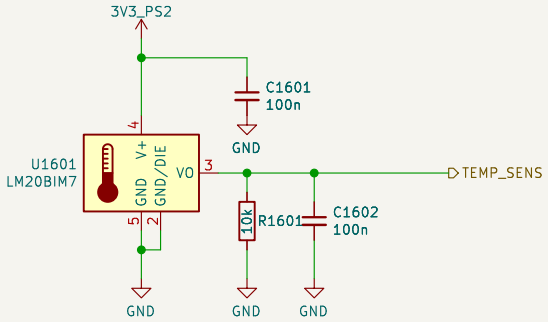
Power EN, Clock, Control, DSP Bus



Misc



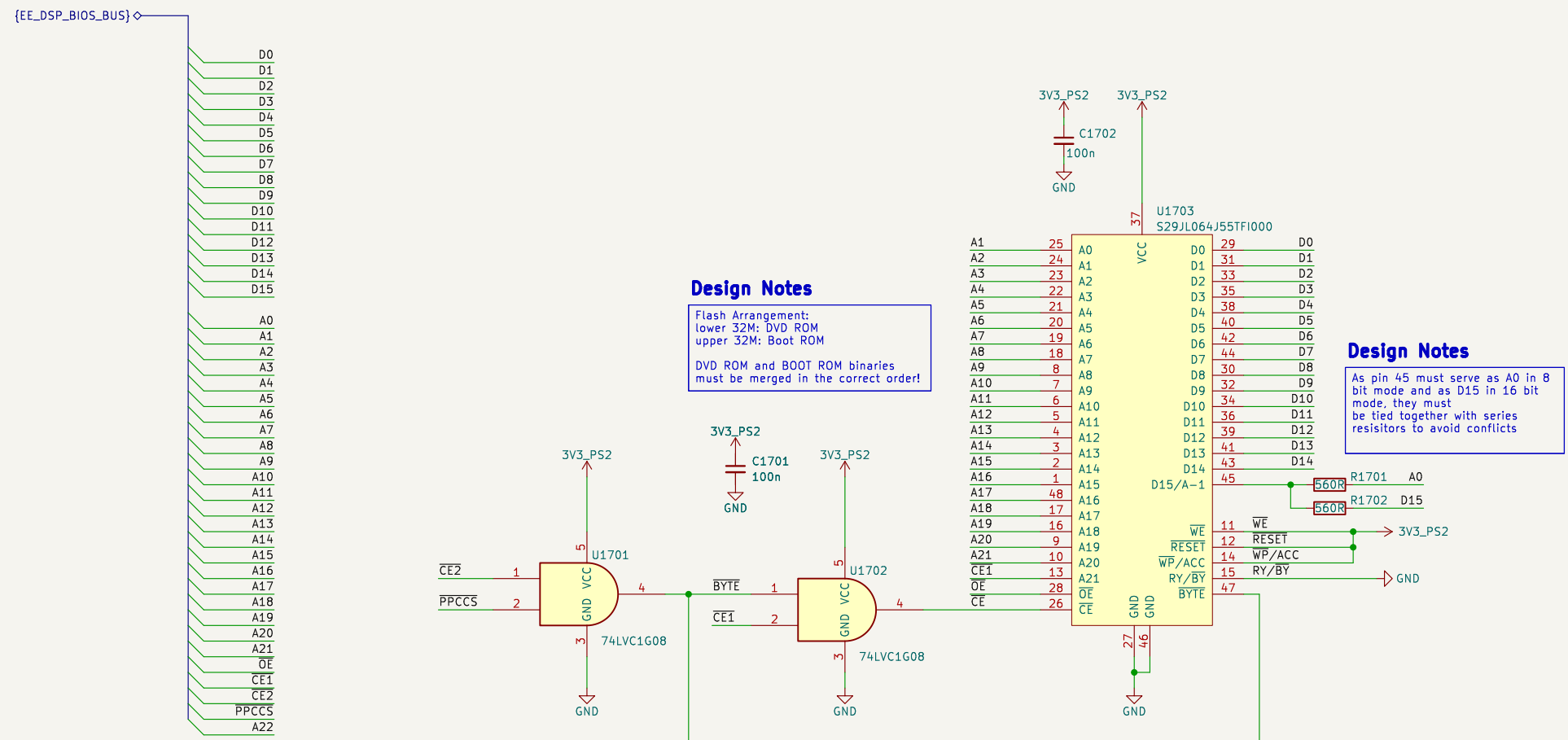
Sheet: /PlayStation 2 – MAIN/Mechacon/
File: MechaCon_Interfaces.kicad_sch
Title: PS2 Mechanics Controller
Size: A3 | Date: | **Rev: 0.3**
KiCad E.D.A. 9.0.0 | Id: 15/30



Sheet: /PlayStation 2 – MAIN/Temperature/
File: PS2_TempSens.kicad_sch

Title: PS2 EE Analog Temperature Sensor

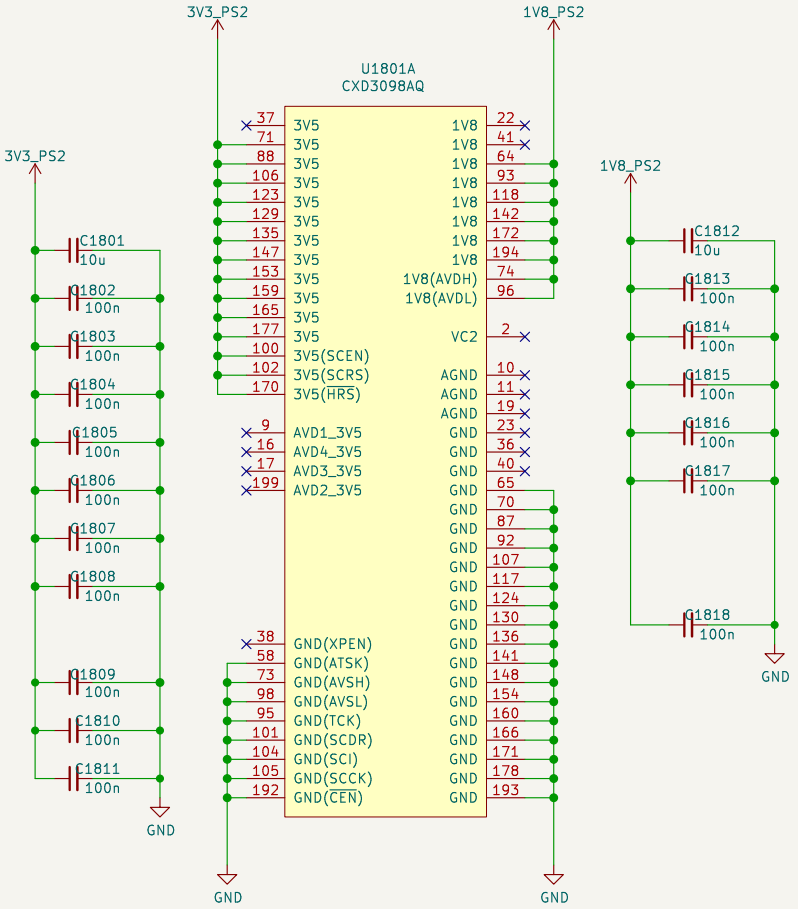
Size: A4	Date:	**Rev: 0.3**
KiCad E.D.A. 9.0.0		Id: 16/30



Sheet: /PlayStation 2 – MAIN/BIOS/
File: PS2_BIOS.kicad_sch

Title: PS2 Boot ROM Flash

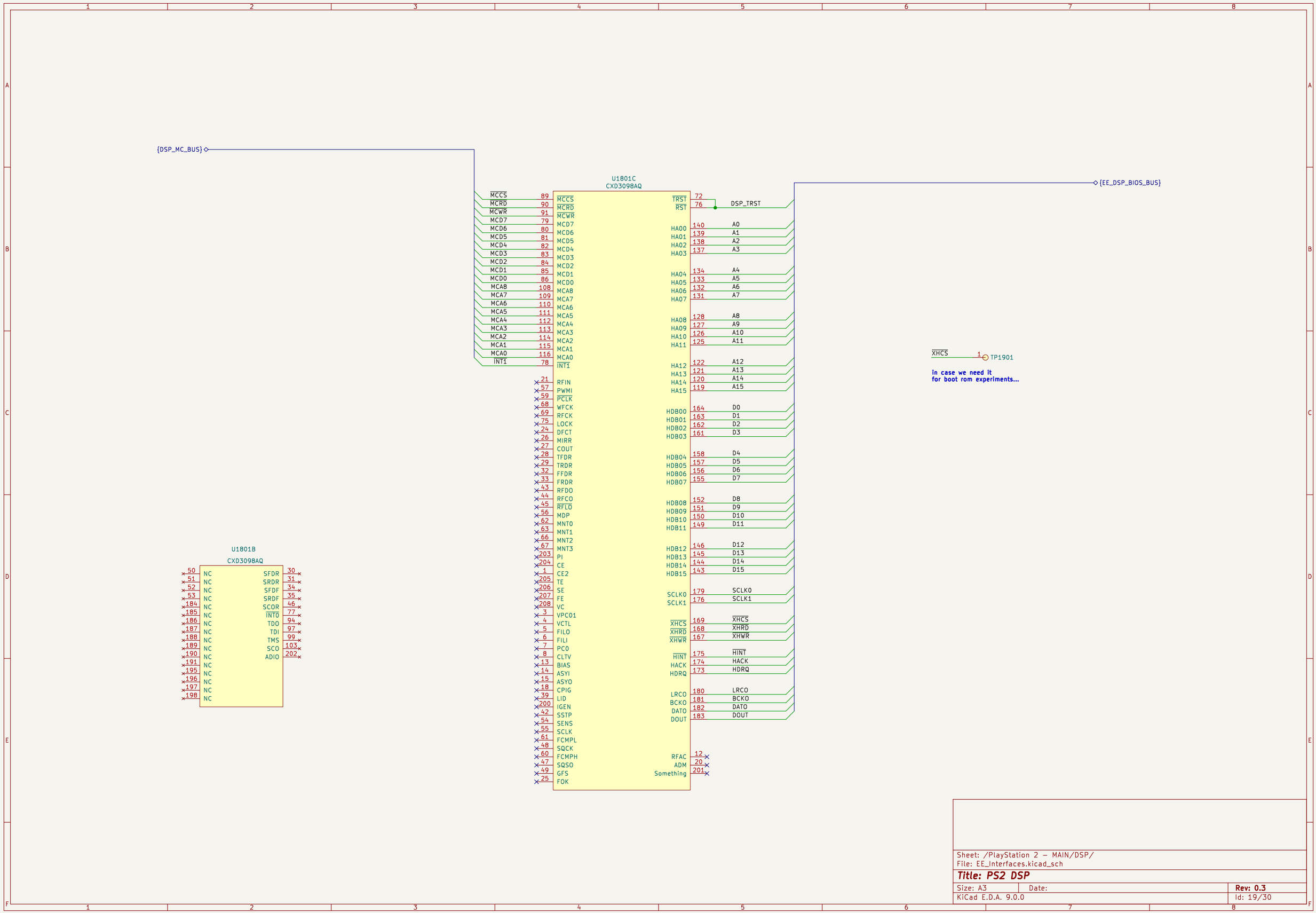
Size: A4	Date:	Rev: 0.3
KiCad E.D.A. 9.0.0		Id: 17/30



Sheet: /PlayStation 2 – MAIN/DSP Power/
File: DSP_Power_Decoupling.kicad_sch

Title: PS2 DSP Power

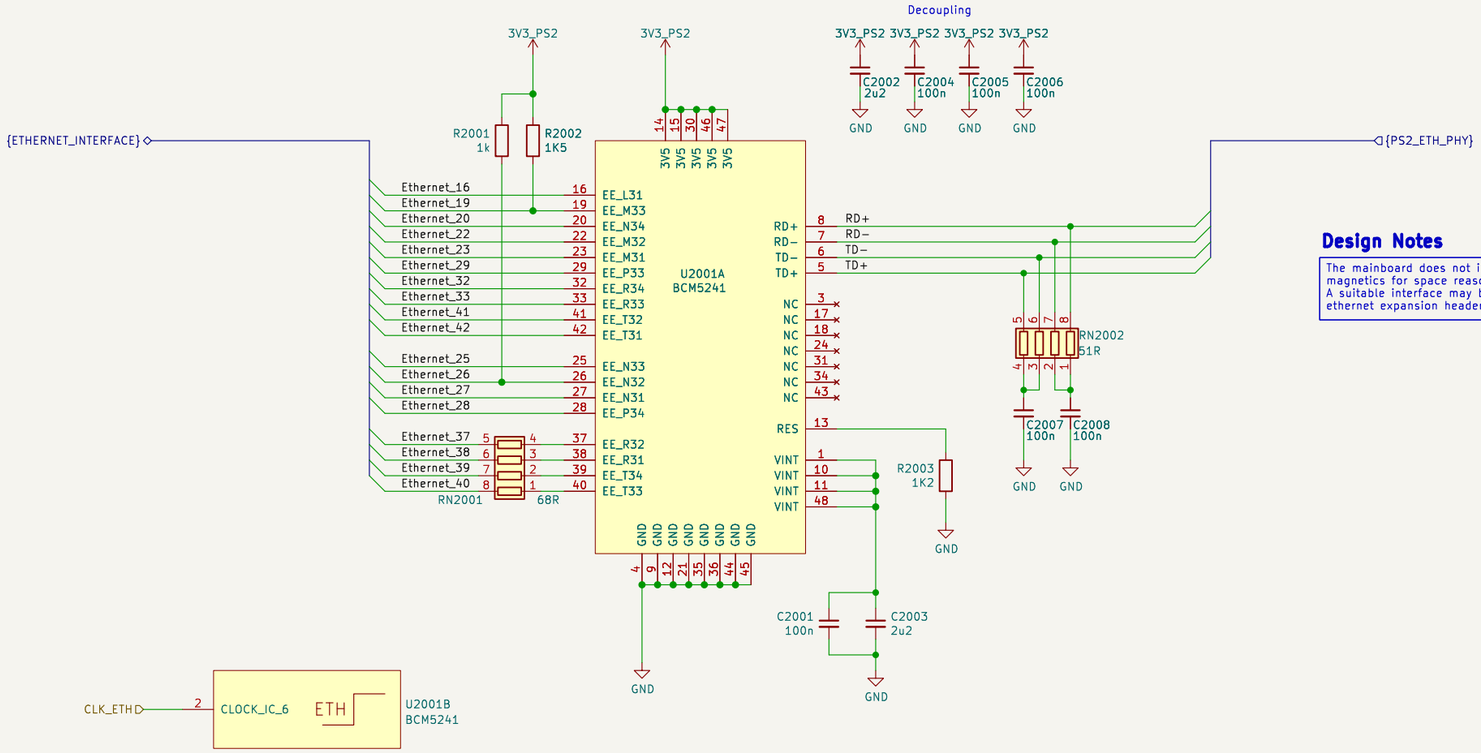
Size: A4	Date:	**Rev: 0.3**
KiCad E.D.A. 9.0.0		Id: 18/30



Sheet: /PlayStation 2 – MAIN/DSP/
File: EE_Interfaces.kicad_sch

Title: PS2 DSP

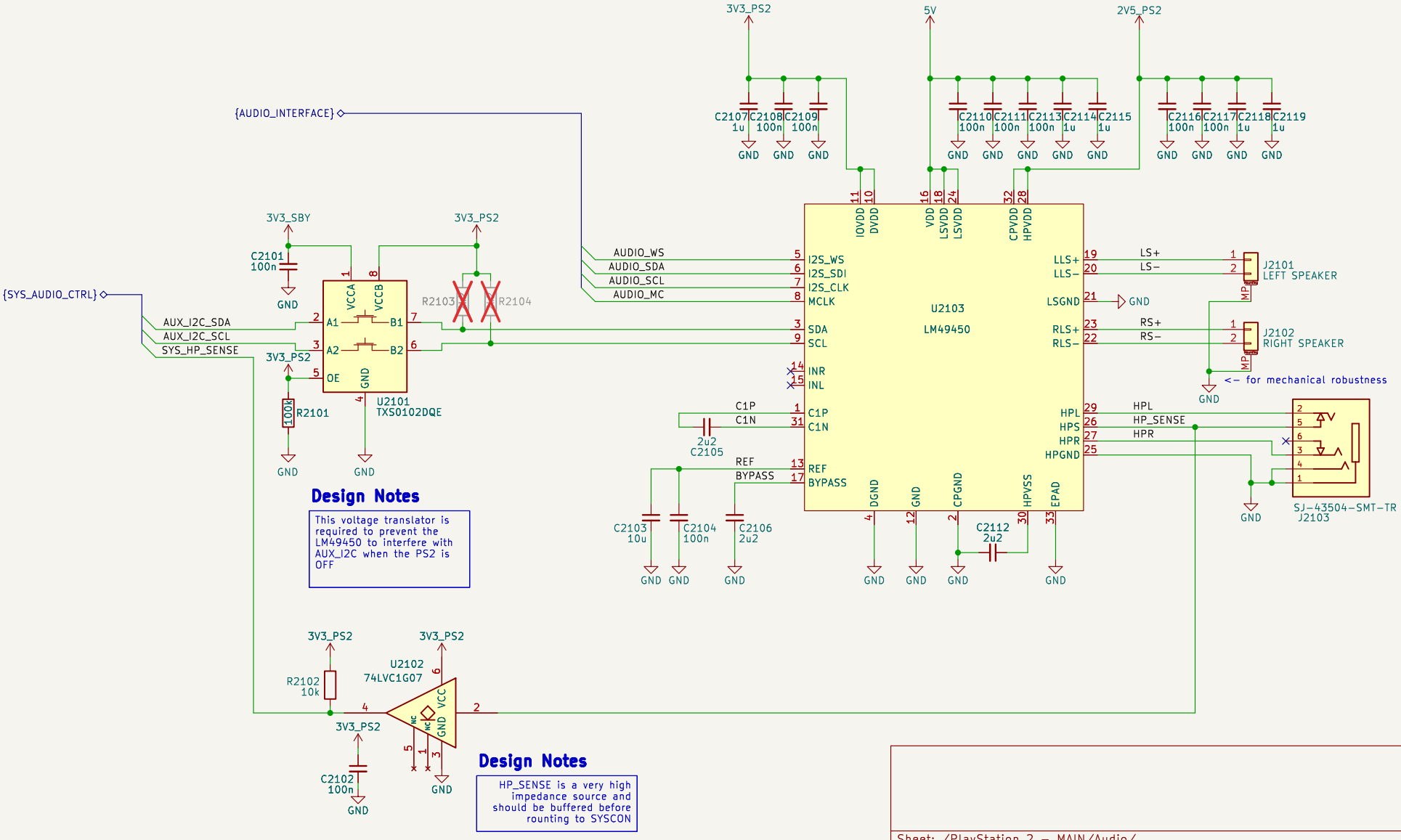
Size: A3	Date:	**Rev: 0.3**
KiCad E.D.A. 9.0.0		Id: 19/30



Sheet: /PlayStation 2 – MAIN/Network/
File: PS2_Network.kicad_sch

Title: PS2 Ethernet PHY

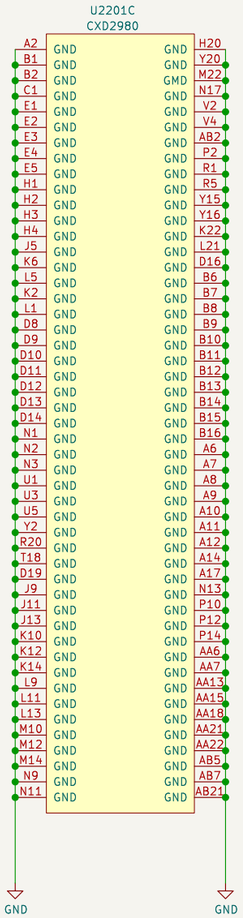
Size: A3	Date:	**Rev: 0.3**
KiCad E.D.A. 9.0.0		Id: 20/30

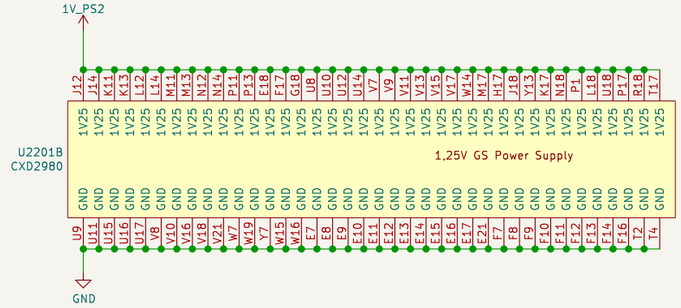


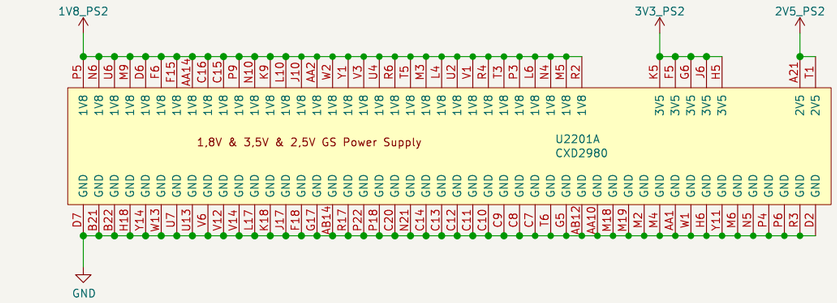
Sheet: /PlayStation 2 – MAIN/Audio/
File: PS2_Audio.kicad_sch

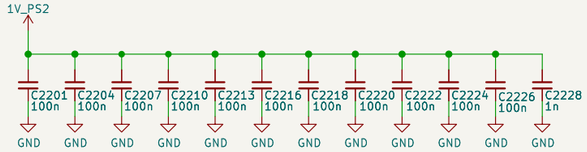
Title: PS2 Audio Codec

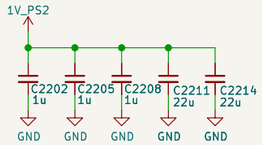
Size: A4	Date:	Rev: 0.3
KiCad E.D.A. 9.0.0		Id: 21/30

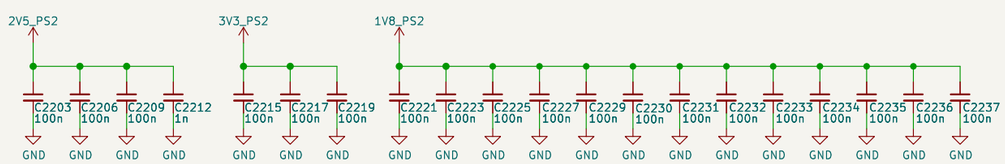










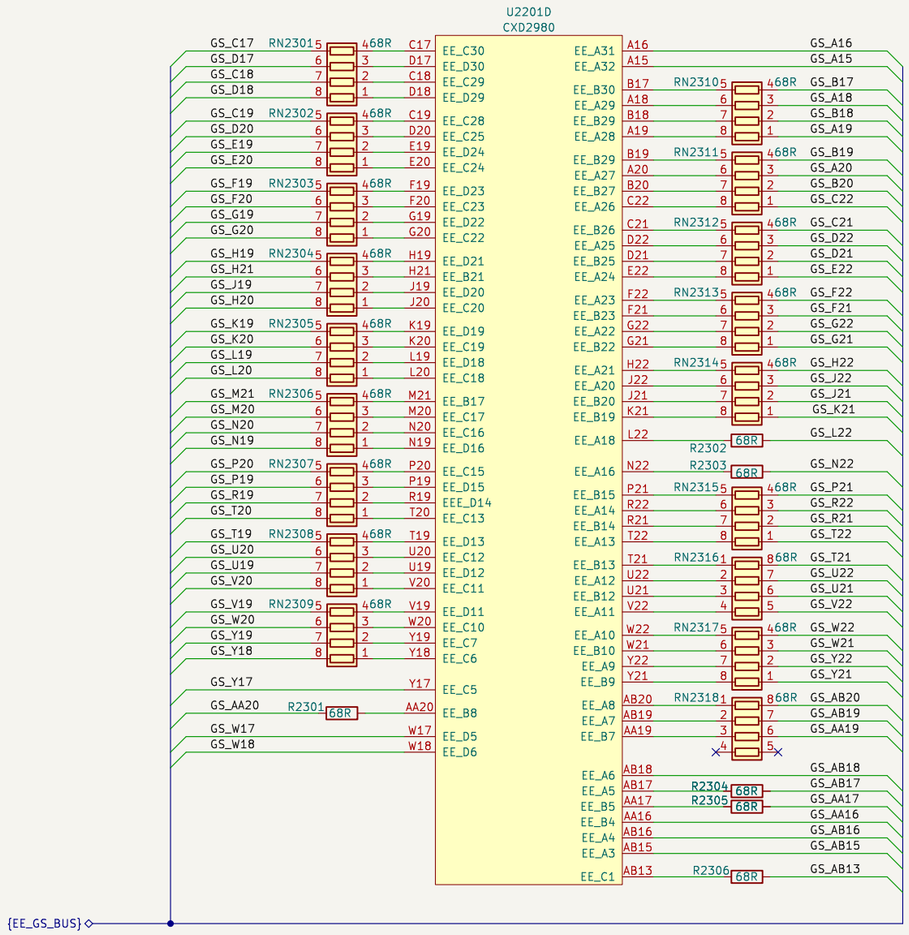


Sheet: /PlayStation 2 – MAIN/Graphics S. Power/
File: GS_Power_Decoupling.kicad_sch

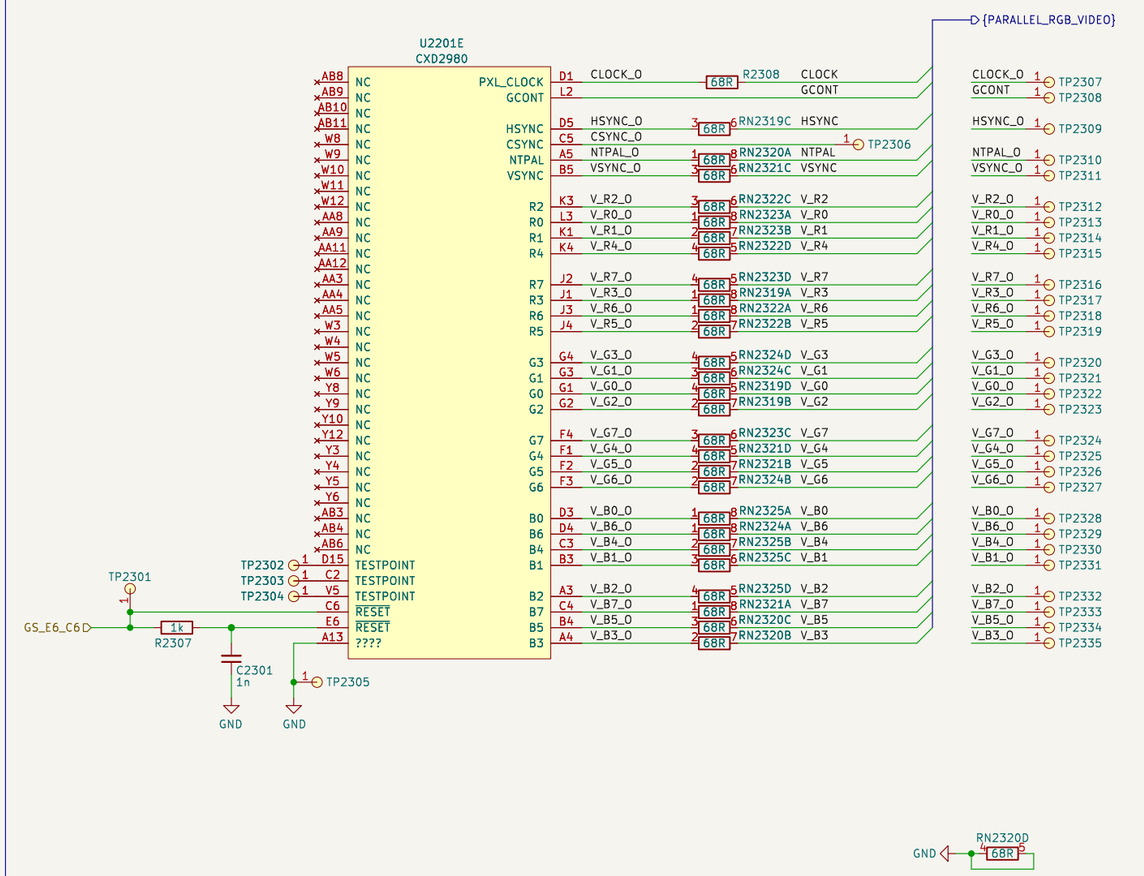
Title: PS2 Graphics Synthesizer Power

Size: A3	Date:	**Rev: 0.3**
KiCad E.D.A. 9.0.0		Id: 22/30

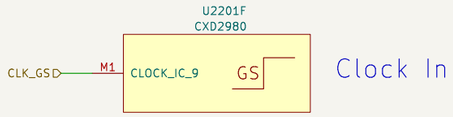
Parallel interface with EE



Parallel video Output and Misc.



Clock In



Sheet: /PlayStation 2 – MAIN/GS/		
File: EE_GS_Interface.kicad_sch		
Title: PS2 Graphics Synthesizer Main		
Size: A3	Date:	**Rev: 0.3**
KiCad E.D.A. 9.0.0		Id: 23/30

To Ports

USB2 is unused, but
exposed on the memory card flex

To EE

{PS2_MC1}
{PS2_MC2}
{PS2_GP1}
{PS2_USB1}
{PS2_USB2}
{FRONT_IO}

3V3_PS2
R2408 1k
R2411 1k

MC1_DAT RN2402D 68R MEMCARD1_DAT
MC1_CLK RN2401C 68R MEMCARD1_CLK
MC1_CMD RN2402C 68R MEMCARD1_CMD
MC1_ATT RN2401D 68R MEMCARD1_ATT
MC1_ACK RN2401B 68R MEMCARD1_ACK

3V3_PS2
R2409 1k
R2412 1k

MC2_DAT RN2403C 68R MEMCARD2_DAT
MC2_CLK RN2404D 68R MEMCARD2_CLK
MC2_CMD RN2403B 68R MEMCARD2_CMD
MC2_ATT RN2403A 68R MEMCARD2_ATT
MC2_ACK RN2404C 68R MEMCARD2_ACK

3V3_PS2
R2401 1k
R2402 1k
R2403 1k
R2404 1k
R2405 1k
R2406 1k

TP2402 TP2403 TP2404 TP2405 TP2406

SYS_GP1_CMD
SYS_GP1_DAT
SYS_GP1_CLK
SYS_GP1_ACK
SYS_GP1_ATT
GP1_?

RN2401A 68R
TP2401

RN2404A 68R GAMEPAD1_CMD
RN2404B 68R GAMEPAD1_DAT
RN2402A 68R GAMEPAD1_CLK
GAMEPAD1_ACK
RN2402B 68R GAMEPAD1_ATT
GAMEPAD1_?

C2401 100p GND
C2402 100p GND
C2403 100p GND

TP2407 GAMEPAD2_CMD
TP2408 GAMEPAD2_DAT
TP2409 GAMEPAD2_CLK
TP2410 GAMEPAD2_ACK
TP2411 GAMEPAD2_ATT
TP2412 GAMEPAD2_?

RN2403D 68R GND GND

USB1_DP USB1_D+
USB1_DN USB1_D−
USB2_DP USB2_D+
USB2_DN USB2_D−

may add 22R series R before pulldown

C2404 100p GND
C2405 100p GND
C2406 100p GND
C2407 100p GND

R2407 15k
R2410 15k
R2413 15k
R2414 15k
GND

Sheet: /PlayStation 2 – MAIN/Front IO/
File: PS2_Front_IO.kicad_sch

Title: PS2 Front IO Filters

Size: A3	Date:	**Rev: 0.3**
KiCad E.D.A. 9.0.0		Id: 24/30

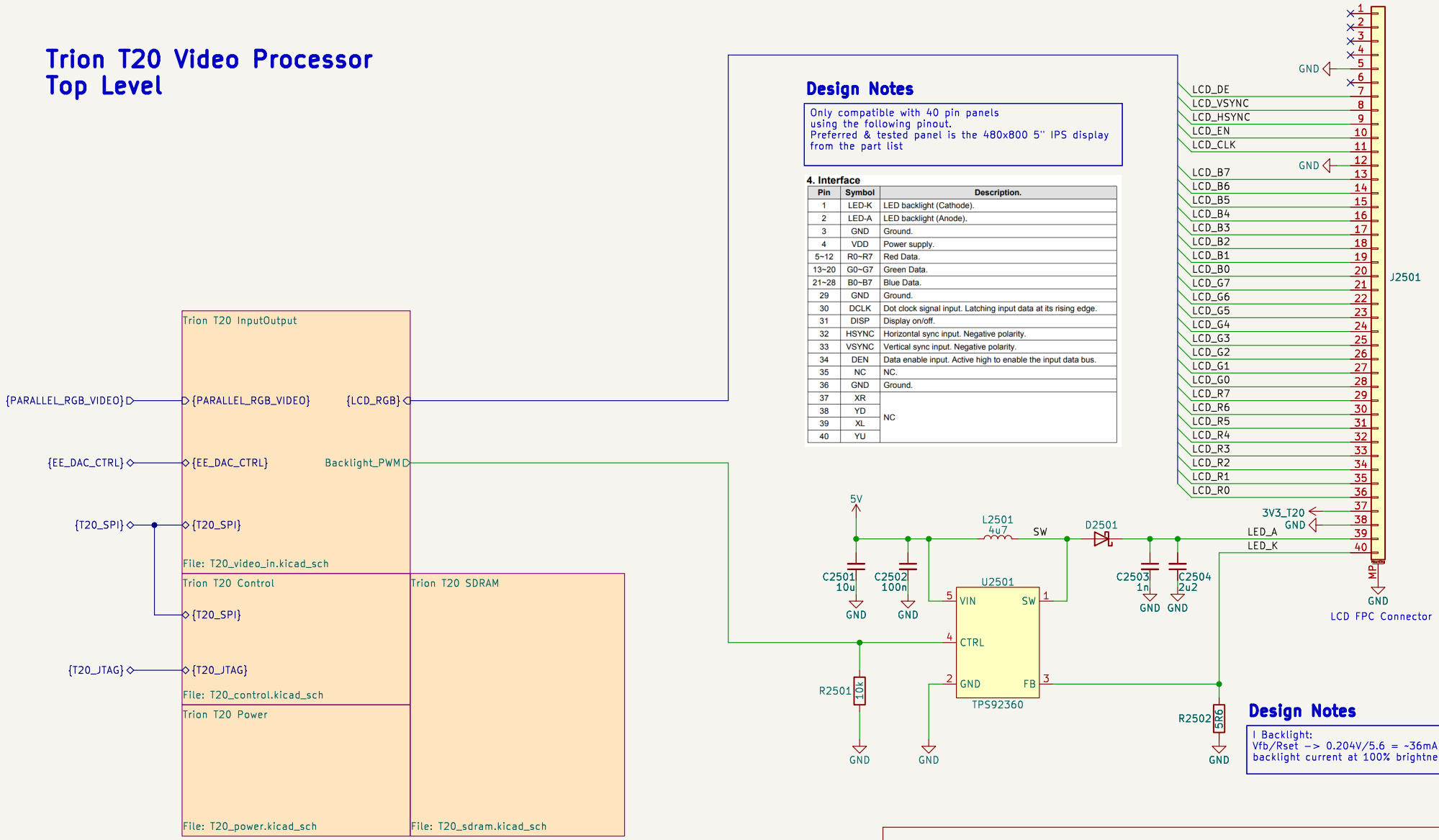
Trion T20 Video Processor
Top Level

Design Notes

Only compatible with 40 pin panels
using the following pinout.
Preferred & tested panel is the 480x800 5'' IPS display
from the part list

4. Interface

Pin	Symbol	Description.
1	LED-K	LED backlight (Cathode).
2	LED-A	LED backlight (Anode).
3	GND	Ground.
4	VDD	Power supply.
5~12	R0~R7	Red Data.
13~20	G0~G7	Green Data.
21~28	B0~B7	Blue Data.
29	GND	Ground.
30	DCLK	Dot clock signal input. Latching input data at its rising edge.
31	DISP	Display on/off.
32	HSYNC	Horizontal sync input. Negative polarity.
33	VSYNC	Vertical sync input. Negative polarity.
34	DEN	Data enable input. Active high to enable the input data bus.
35	NC	NC.
36	GND	Ground.
37	XR	NC
38	YD	
39	XL	
40	YU	



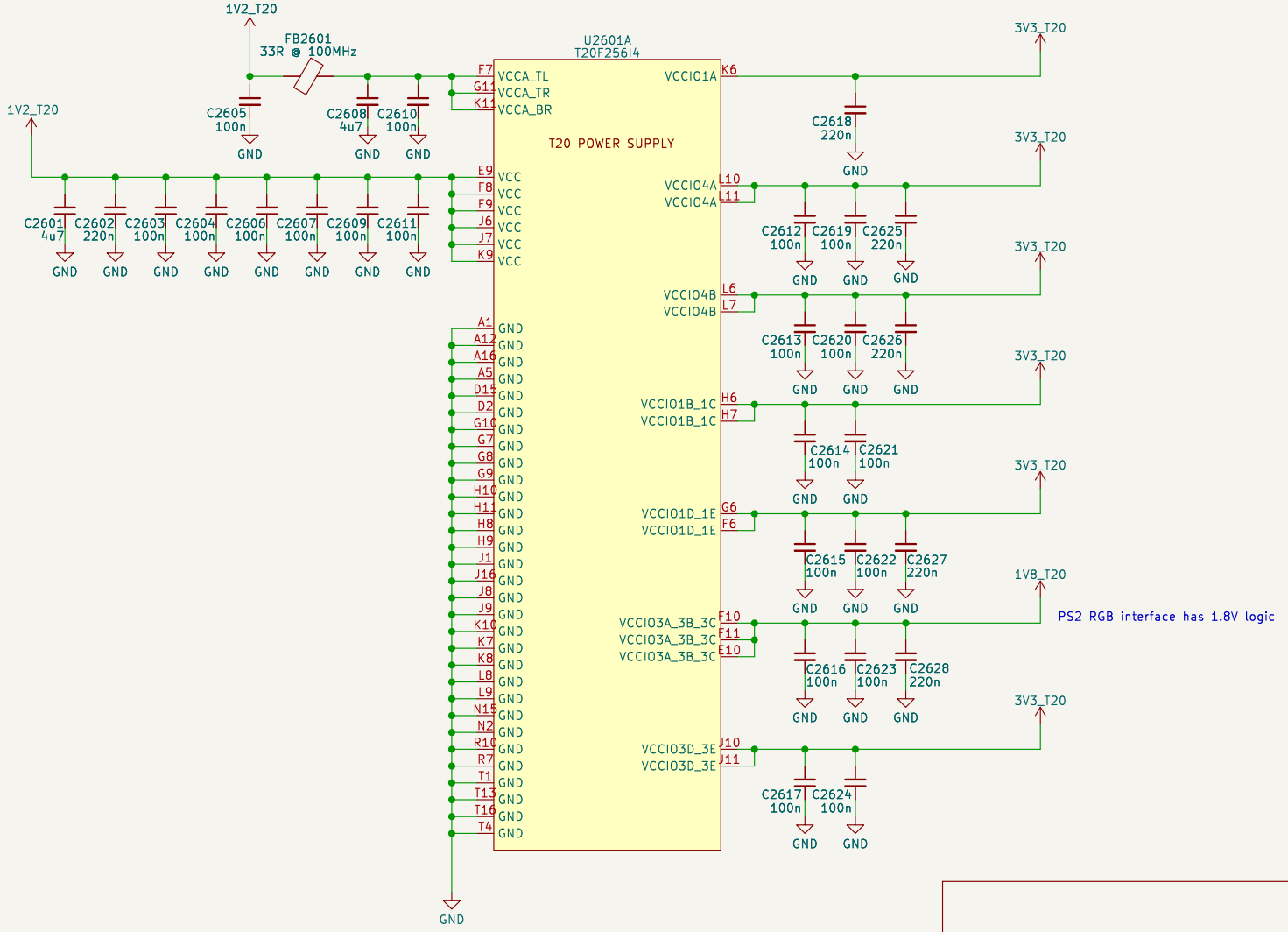
Design Notes

I Backlight:
Vfb/Rset -> 0.204V/5.6 = ~36mA
backlight current at 100% brightness

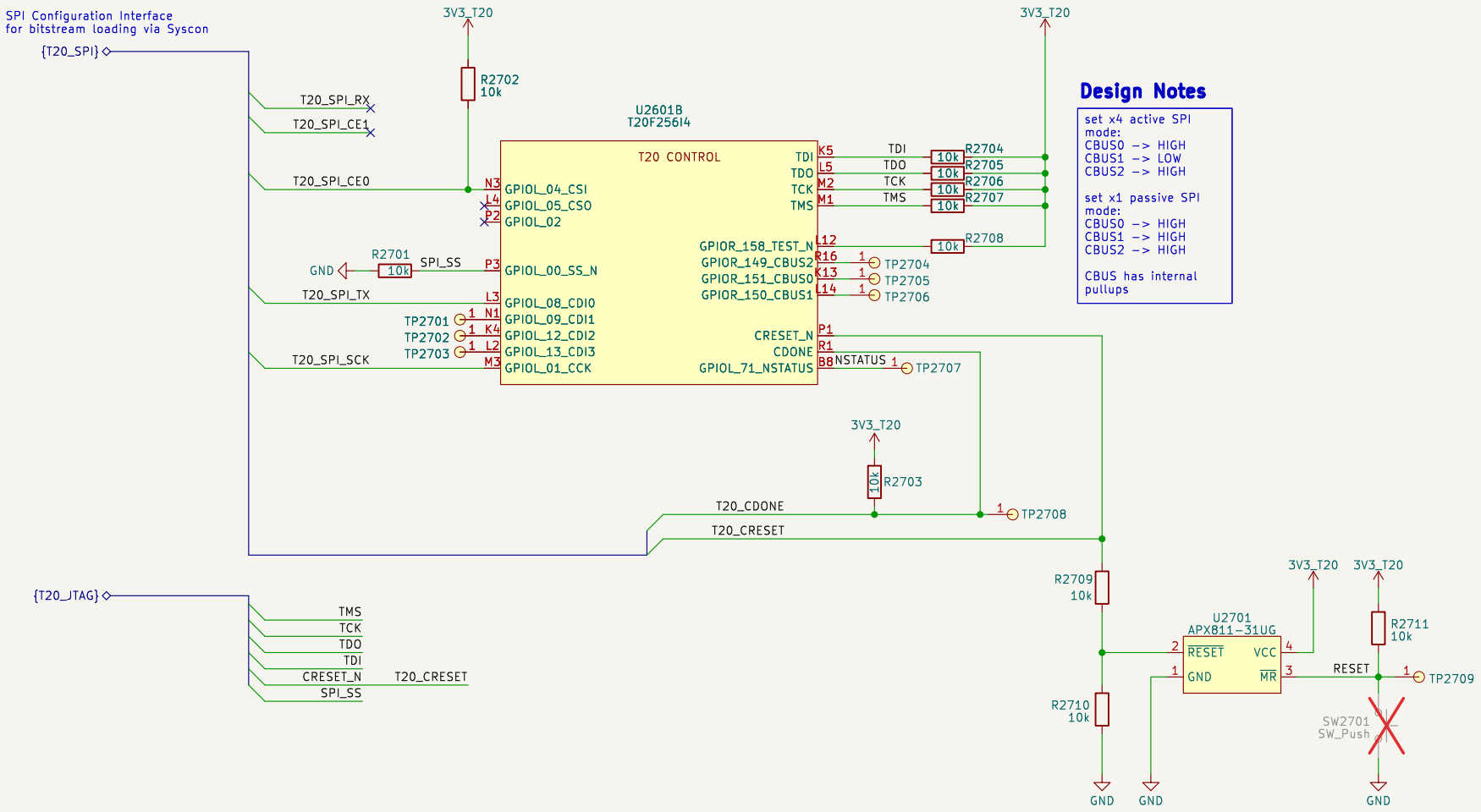
Sheet: /Video Processor/
File: Trion_T20.kicad_sch

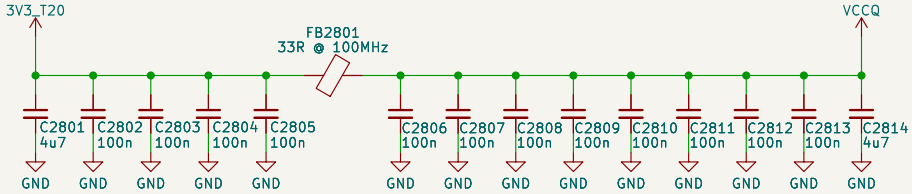
Title: PS2 Video Processor Top Level

Size: A4	Date:	**Rev: 0.3**
KiCad E.D.A. 9.0.0		Id: 25/30



Sheet: /Video Processor/Trion T20 Power/	
File: T20_power.kicad_sch	
Title: PS2 Video Processor Power	
Size: A4	Date:
KiCad E.D.A. 9.0.0	Rev: 0.3
	Id: 26/30

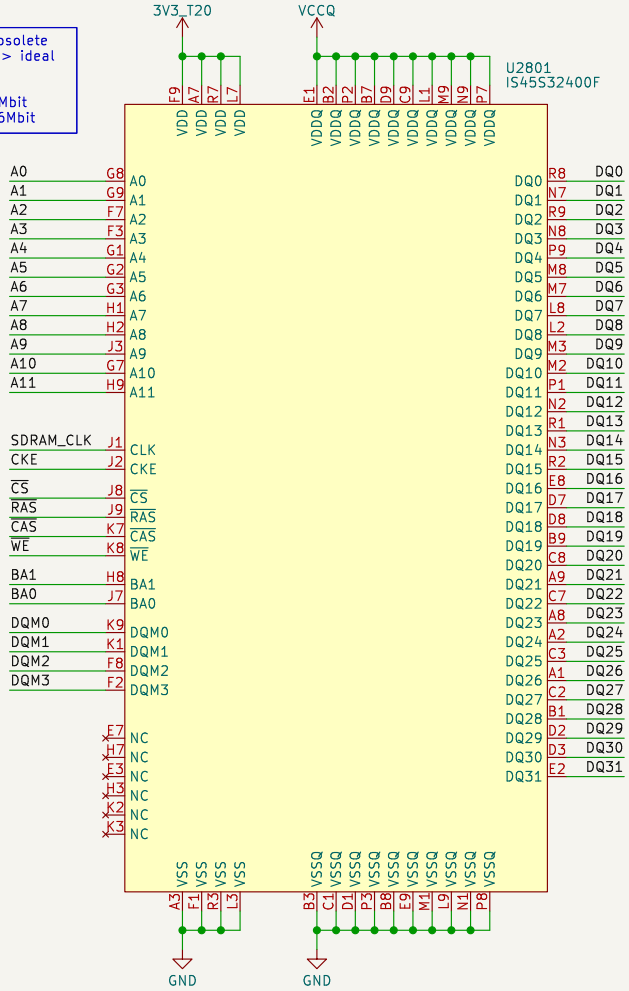

SPI Configuration Interface
for bitstream loading via Syscon
{T20_SPI}
T20_SPI_RX
T20_SPI_CE1
T20_SPI_CE0
T20_SPI_TX
T20_SPI_SCK
3V3_T20
R2702
10k
U2601B
T20F256I4
T20 CONTROL
GPIOL_04_CSI
GPIOL_05_CSO
GPIOL_02
GPIOL_00_SS_N
GPIOL_08_CDI0
GPIOL_09_CDI1
GPIOL_12_CDI2
GPIOL_13_CDI3
GPIOL_01_CCK
TDI
TDO
TCK
TMS
GPIOR_158_TEST_N
GPIOR_149_CBUS2
GPIOR_151_CBUS0
GPIOR_150_CBUS1
CRESET_N
CDONE
GPIOL_71_NSTATUS
R2704
R2705
R2706
R2707
R2708
TP2704
TP2705
TP2706
TP2707
R2701
SPI_SS
GND
TP2701
TP2702
TP2703
R2703
T20_CDONE
T20_CRESET
TP2708
Design Notes
set x4 active SPI mode:
CBUS0 -> HIGH
CBUS1 -> LOW
CBUS2 -> HIGH
set x1 passive SPI mode:
CBUS0 -> HIGH
CBUS1 -> HIGH
CBUS2 -> HIGH
CBUS has internal pullups
{T20_JTAG}
TMS
TCK
TDO
TDI
CRESET_N
SPI_SS
T20_CRESET
R2709
R2710
U2701
APX811-31UG
RESET
VCC
GND
MR
R2711
TP2709
SW2701
SW_Push
Sheet: /Video Processor/Trion T20 Control/
File: T20_control.kicad_sch
Title: PS2 Video Processor Control & Debug
Size: A4
Date:
Rev: 0.3
KiCad E.D.A. 9.0.0
Id: 27/30

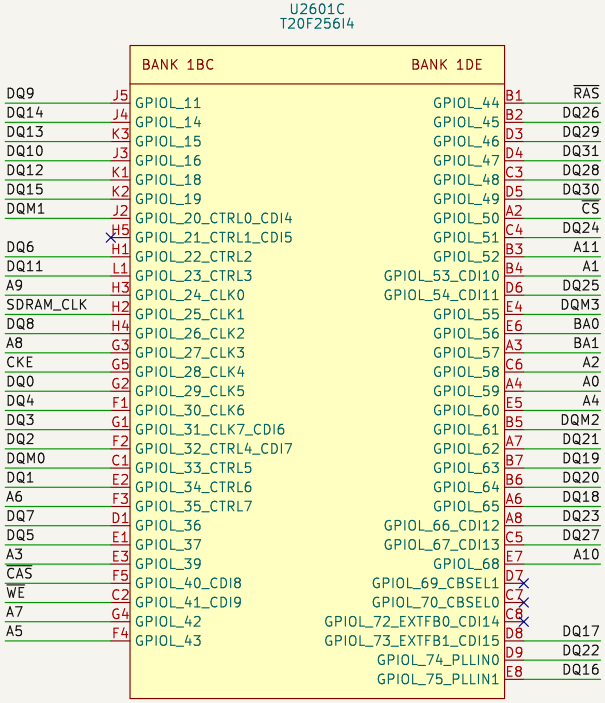


Design Notes

ORIGINAL: IS42S32400F-6BL -> obsolete
ALTERNATIVES: IS42S32400J-6BL -> ideal

Others(pin to pin compatible)
AS4C4M32S-6BIN -> 166MHz 128Mbit
IS42S32800J-6BLI -> 166MHz 256Mbit





Sheet: /Video Processor/Trion T20 SDRAM/
File: T20_sdram.kicad_sch

Title: PS2 Video Processor Framebuffer

Size: A4	Date:	Rev: 0.3
KiCad E.D.A. 9.0.0		Id: 28/30

Video Processor Input/Output Block

{PARALLEL_RGB_VIDEO}

Parallel Video Input
from PS2 GS
RX only

CLOCK
GCONT
HSYNC
CSYNC
NTPAL
VSYNC
V_R2
V_R0
V_R1
V_R4
V_R7
V_R3
V_R6
V_R5
V_G3
V_G1
V_G0
V_G2
V_G7
V_G4
V_G5
V_G6
V_B0
V_B6
V_B4
V_B1
V_B2
V_B7
V_B5
V_B3

{EE_DAC_CTRL}

Control interface
from PS2 EE
RX only

DAC_RST
DAC_SCL
DAC_SDA

{T20_SPI}

Control interface
from/to Syscon

T20_SPI_SCK
T20_SPI_TX
T20_SPI_RX
T20_SPI_CE0
T20_CDONE
T20_CRESET
T20_SPI_CE1

U2601D
T20F256I4

BANK3ABC

C9	GPIOR_76_PLLIN0	
D10	GPIOR_77_PLLIN1	
A9	GPIOR_78_EXTFB0_CDI31	V_B2
A10	GPIOR_79_EXTFB1_CDI30	V_B3
B9	GPIOR_80	NTPAL
C10	GPIOR_81_MREFCLK	
B10	GPIOR_82	V_B5
B11	GPIOR_83	V_B4
A11	GPIOR_84	V_B1
C12	GPIOR_85	V_G1
C11	GPIOR_86	V_B6
D11	GPIOR_87_CDI29	V_G6
E11	GPIOR_88_CDI28	
D12	GPIOR_89	V_R5
C14	GPIOR_102	V_R6
D13	GPIOR_103	V_R4
D14	GPIOR_104_CDI25	V_R2
E13	GPIOR_105_CDI24	
B16	GPIOR_106	HSYNC
A14	GPIOR_90	V_G5
E12	GPIOR_91	
B14	GPIOR_92	V_B7
B12	GPIOR_93	V_B0
A15	GPIOR_94_CDI27	V_G0
A13	GPIOR_95_CDI26	V_G4
B13	GPIOR_97	VSYNC
B15	GPIOR_98	V_G2
C13	GPIOR_99	V_G3
C16	GPIOR_108	V_R3
E14	GPIOR_110	
E16	GPIOR_111	
C15	GPIOR_112_CDI23	V_R7
F13	GPIOR_113_CDI22	
D16	GPIOR_116_CTRL15	
G13	GPIOR_117_CTRL14	
F14	GPIOR_118_CTRL13	
E16	GPIOR_119_CTRL12	V_R1
E15	GPIOR_120_CLK15	V_G7
G12	GPIOR_121_CLK14	
F15	GPIOR_122_CLK13_CDI21	V_R0
F16	GPIOR_123_CLK12_CDI20	CLOCK

BANK 3DE

G15	GPIOR_124_CLK11	DAC_SCL 1 TP2901
H13	GPIOR_125_CLK10	CLK_50MHz
G16	GPIOR_126_CLK9	
G14	GPIOR_127_CLK8	T20_SPI_SCK 1 TP2902
H14	GPIOR_128_CTRL11	
H15	GPIOR_129_CTRL10	DAC_SDA 1 TP2903
H16	GPIOR_130_CTRL9	DAC_RST 1 TP2904
J15	GPIOR_131_CTRL8	T20_SPI_TX 1 TP2905
K16	GPIOR_132_CDI19	T20_SPI_RX 1 TP2906
J13	GPIOR_133_CDI18	T20_SPI_CE1
J14	GPIOR_135_CDI17	
K15	GPIOR_136_CDI16	
K14	GPIOR_138	
H12	GPIOR_139	
J12	GPIOR_141	
L16	GPIOR_143	
M15	GPIOR_144	
M16	GPIOR_145	
P16	GPIOR_146	
L15	GPIOR_147	
K12	GPIOR_148	
N14	GPIOR_153	
N16	GPIOR_154	
P15	GPIOR_155	
M14	GPIOR_156	
L13	GPIOR_157_PLLIN	CLK_50MHz

Backlight_PWM
{LCD_RGB}

To LCD and Backlight Driver

U2601E
T20F256I4

BANK4A

M13	GPIOB_CLKN0	
M12	GPIOB_CLKP0	
P9	GPIOB_RXN00	
M9	GPIOB_RXN01	
T10	GPIOB_RXN02	LCD_B2
N10	GPIOB_RXN03	
R11	GPIOB_RXN04	LCD_B4
M11	GPIOB_RXN05	LCD_DE
P11	GPIOB_RXN06	
R12	GPIOB_RXN07	LCD_B6
P13	GPIOB_RXN08	
R14	GPIOB_RXN09	LCD_CLK
N12	GPIOB_RXN10	
R15	GPIOB_RXN11	LCD_HSYNC
N13	GPIOB_RXN12_EXTFB0	
P9	GPIOB_RXP00	
N9	GPIOB_RXP01	
T9	GPIOB_RXP02	LCD_B1
P10	GPIOB_RXP03	
T11	GPIOB_RXP04	LCD_B3
M10	GPIOB_RXP05	LCD_VSYNC
N11	GPIOB_RXP06	
T12	GPIOB_RXP07	LCD_B5
R13	GPIOB_RXP08	
T14	GPIOB_RXP09	LCD_B7
P12	GPIOB_RXP10	
T15	GPIOB_RXP11	LCD_EN
X14	GPIOB_RXP12_EXTFB0	

BANK4B

M5	GPIOB_TXN00	LCD_G0
P4	GPIOB_TXN01	LCD_R5
R4	GPIOB_TXN02	LCD_R2
T3	GPIOB_TXN03	LCD_R3
P5	GPIOB_TXN04	
M7	GPIOB_TXN05	LCD_G2
P6	GPIOB_TXN06	
T5	GPIOB_TXN07	LCD_G4
T6	GPIOB_TXN08	LCD_G6
P7	GPIOB_TXN09	
T7	GPIOB_TXN10	LCD_G7
N8	GPIOB_TXN11	
P8	GPIOB_TXN12	
M4	GPIOB_TXP00	LCD_R6
N4	GPIOB_TXP01	LCD_R4
R3	GPIOB_TXP02	LCD_R0
T2	GPIOB_TXP03	LCD_R1
N5	GPIOB_TXP04	LCD_R7
M6	GPIOB_TXP05	LCD_G1
N6	GPIOB_TXP06	
R5	GPIOB_TXP07	LCD_G3
R6	GPIOB_TXP08	LCD_G5
N7	GPIOB_TXP09	
T8	GPIOB_TXP10	LCD_B0
M8	GPIOB_TXP11	
P8	GPIOB_TXP12	
R2	REF_RES	REF_RES

R2902
12k
GND

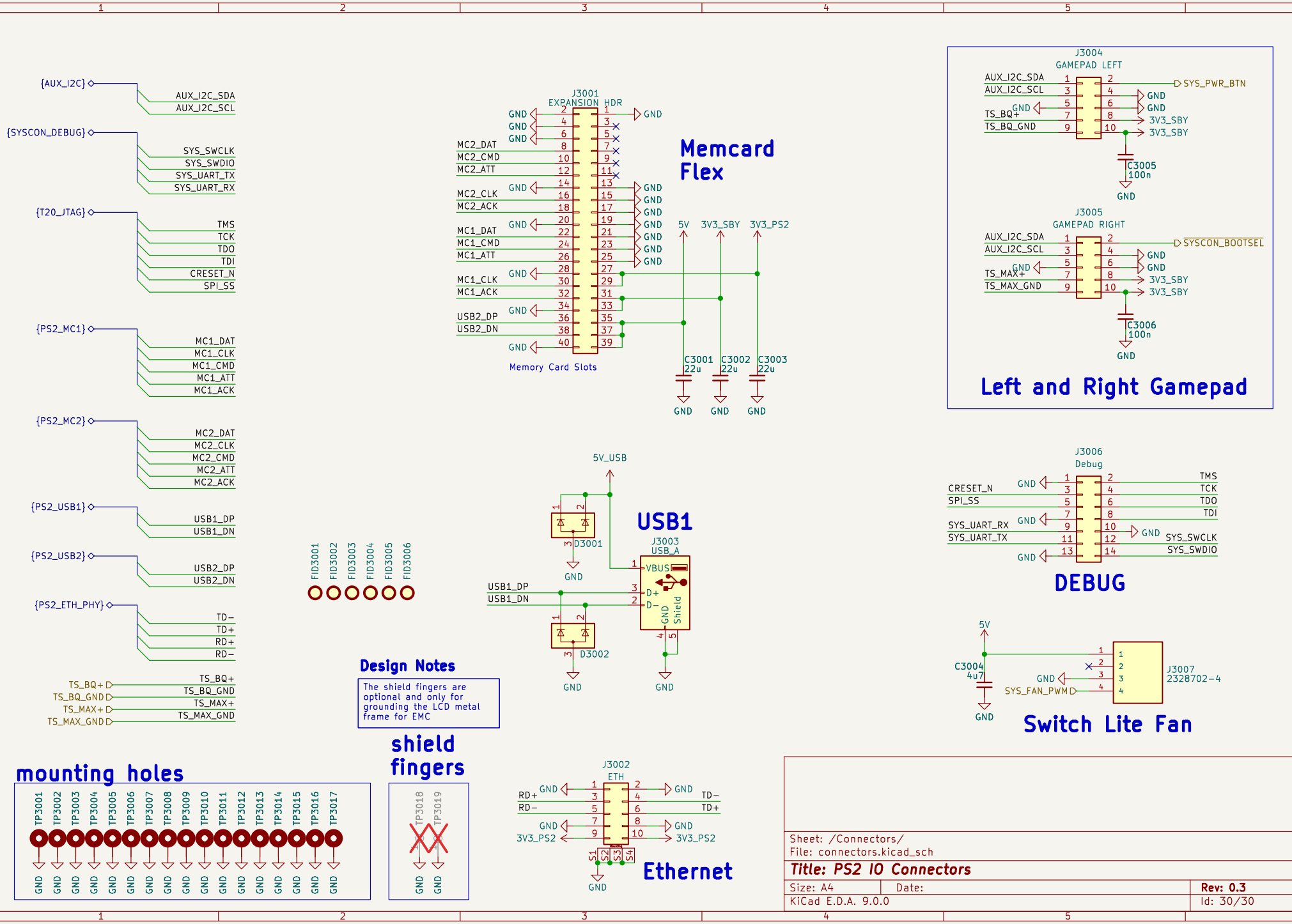
Main FPGA Clock
-> 50MHz Input to PLL

3V3_T20
FB2901
33R @ 100MHz
C2901
470n
C2902
470n
C2903
100n
GND
X2901
ASE-50MHz
Vdd
EN
OUT
R2901
22R
CLK_50MHz

Sheet: /Video Processor/Trion T20 InputOutput/
File: T20_video_in.kicad_sch

Title: PS2 Video Processor Video In & Out

Size: A3	Date:	**Rev: 0.3**
KiCad E.D.A. 9.0.0		Id: 29/30


{AUX_I2C}
AUX_I2C_SDA
AUX_I2C_SCL
{SYSCON_DEBUG}
SYS_SWCLK
SYS_SWDIO
SYS_UART_TX
SYS_UART_RX
{T20_JTAG}
TMS
TCK
TDO
TDI
CRESET_N
SPI_SS
{PS2_MC1}
MC1_DAT
MC1_CLK
MC1_CMD
MC1_ATT
MC1_ACK
{PS2_MC2}
MC2_DAT
MC2_CLK
MC2_CMD
MC2_ATT
MC2_ACK
{PS2_USB1}
USB1_DP
USB1_DN
{PS2_USB2}
USB2_DP
USB2_DN
{PS2_ETH_PHY}
TD−
TD+
RD+
RD−
TS_BQ+
TS_BQ_GND
TS_MAX+
TS_MAX_GND
J3001
EXPANSION HDR
Memcard Flex
Memory Card Slots
C3001 22u
C3002 22u
C3003 22u
5V
3V3_SBY
3V3_PS2
J3004
GAMEPAD LEFT
SYS_PWR_BTN
C3005 100n
J3005
GAMEPAD RIGHT
SYSCON_BOOTSEL
C3006 100n
Left and Right Gamepad
J3006
Debug
DEBUG
FID3001
FID3002
FID3003
FID3004
FID3005
FID3006
5V_USB
USB1
J3003
USB_A
D3001
D3002
Design Notes
The shield fingers are optional and only for grounding the LCD metal frame for EMC
shield fingers
TP3018
TP3019
mounting holes
TP3001
TP3002
TP3003
TP3004
TP3005
TP3006
TP3007
TP3008
TP3009
TP3010
TP3011
TP3012
TP3013
TP3014
TP3015
TP3016
TP3017
J3002
ETH
Ethernet
C3004 4u7
J3007 2328702-4
SYS_FAN_PWM
Switch Lite Fan
Sheet: /Connectors/
File: connectors.kicad_sch
Title: PS2 IO Connectors
Size: A4
Date:
Rev: 0.3
KiCad E.D.A. 9.0.0
Id: 30/30